

# DATA SHEET

## **SAA5246A**

### **Integrated VIP and Teletext (IVT1.0)**

Product specification  
Supersedes data of August 1992  
File under Integrated Circuits, IC02

January 1993

## Integrated VIP and Teletext (IVT1.0)

## SAA5246A

### FEATURES

- Complete Teletext decoder in a 48-pin DIL or 64-pin QFP, integrated circuit
- Single +5 V power supply
- Both video and scan related synchronization modes are supported
- RGB interface to standard colour decoder ICs, push-pull output drive
- Digital data slicer and display clock phase-locked loop reduce peripheral components to a minimum
- Data capture performance similar to SAA5231 (VIP2)
- Option for up to seven national languages
- Optional storage of packet 24 in the display memory
- Separate text and video signal quality detectors, 625/525 video status and language version all readable via I<sup>2</sup>C-bus
- Automatic  $\overline{\text{ODD}}$ /EVEN output control with override
- Control of display PLL free-run and rolling header via I<sup>2</sup>C-bus
- VCS to SCS mode for stable 525 line status display.



### DESCRIPTION

The SAA5246A is a single-chip teletext decoder IC for decoding 625 line base World System Teletext transmissions. The teletext decoder hardware is based on the Enhanced Computer Controlled ECCT device (SAA5243) with some additional features.

The Video Input Processor section of the device uses mixed analog and digital designs in the data slicer and clock phase-locked-loop functions. As a result the number of external components are greatly reduced and no critical or adjustable components are required.

### QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>DD</sub>	positive supply voltage	4.5	5.0	5.5	V
I <sub>DD</sub>	supply current	–	64	128	mA
V <sub>syn</sub>	sync amplitude	0.1	0.3	0.6	V
V <sub>vid</sub>	video amplitude	0.7	1.0	1.4	V
f <sub>X TAL</sub>	crystal frequency	–	27	–	MHz
T <sub>amb</sub>	operating ambient temperature	–20	–	+70	°C

### ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA5246AP	48	DIL	plastic	SOT240AC3 <sup>(1)</sup>
SAA5246AGP	64	QFP	plastic	SOT319DA3 <sup>(2)</sup>

### Notes

1. SOT240-1; 1996 November 22.
2. SOT319-3; 1996 November 22.

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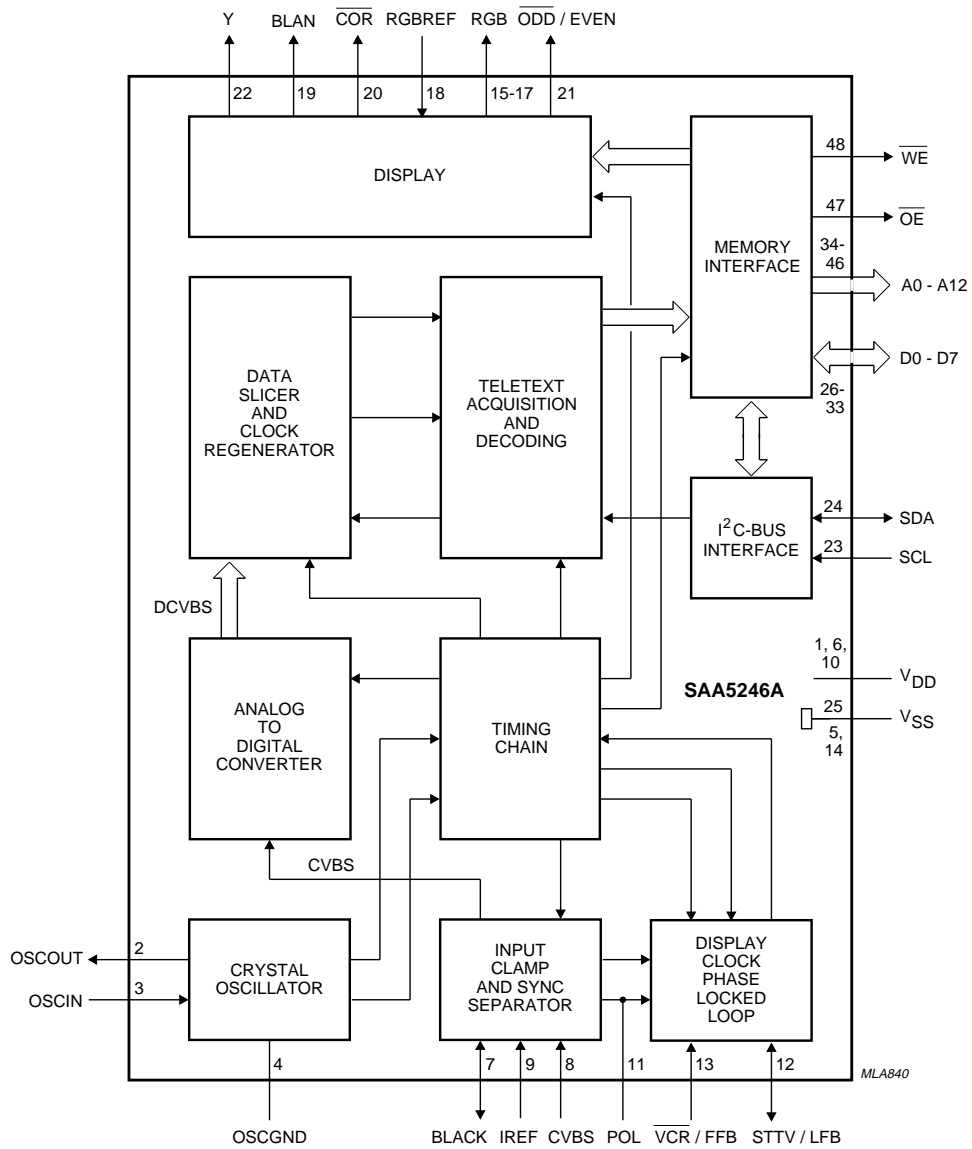


Fig.1 Block diagram for SOT240 (DIL48) package.

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## PINNING

SYMBOL	PIN		DESCRIPTION
	SOT240	SOT319	
OSCOUT	2	27	27 MHz crystal oscillator output
OSCIN	3	28	27 MHz crystal oscillator input
OSCGND	4	29	0 V crystal oscillator ground
V <sub>SS</sub>	5, 14, 25	26, 30, 31, 43, 58	0 V ground
BLACK	7	35	video black level storage pin, connected to ground via a 100 nF capacitor
CVBS	8	36	composite video input pin. A positive-going 1 V (peak-to-peak) input is required, connected via a 100 nF capacitor
IREF	9	37	reference current input pin, connected to ground via a 27 k $\Omega$ resistor
V <sub>DD</sub>	1, 6, 10	25, 32, 38	+5 V positive supply
POL	11	39	STTV/LFB/FFB polarity selection pin
STTV/LFB	12	40	sync to TV output pin/line flyback input pin. Function controlled by an internal register bit (scan sync mode)
VCR/FFB	13	42	PLL time constant switch/field input pin. Function controlled by an internal register bit (scan sync mode)
R	15	44	dot rate character output of the RED colour information
G	16	45	dot rate character output of the GREEN colour information
B	17	47	dot rate character output of the BLUE colour information
RGBREF	18	48	input DC voltage to define the output high level on the RGB pins
BLAN	19	52	dot rate fast blanking output
COR	20	53	programmable output to provide contrast reduction of the TV picture for mixed text and picture displays or when viewing newsflash/subtitle pages. Open-drain output
ODD/EVEN	21	54	a 25 Hz output synchronized to the input CVBS field sync pulses to make a non-interlaced display by adjustment of the vertical deflection currents.
Y	22	55	dot rate character output of teletext foreground colour information. Open-drain output
SCL	23	56	serial clock input for I <sup>2</sup> C-bus. It can still be driven HIGH during power-down of the device
SDA	24	57	serial data port for the I <sup>2</sup> C-bus. Open drain output. It can still be driven HIGH during power-down of the device
D0-D5	26-31	60-64, 3	data ports for the page SRAM
n.c.	–	1, 2, 10, 11, 15, 18, 33, 34, 41, 46, 49 - 51, 59	not connected
D6-D7	32, 33	4, 5	data ports for the page SRAM

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SYMBOL	PIN		DESCRIPTION
	SOT240	SOT319	
A0-A12	34-46	6-9, 12-14, 16, 17, 19-22	address output for the page SRAM
$\overline{\text{OE}}$	47	23	output enable for the page SRAM
$\overline{\text{WE}}$	48	24	write enable for the page SRAM

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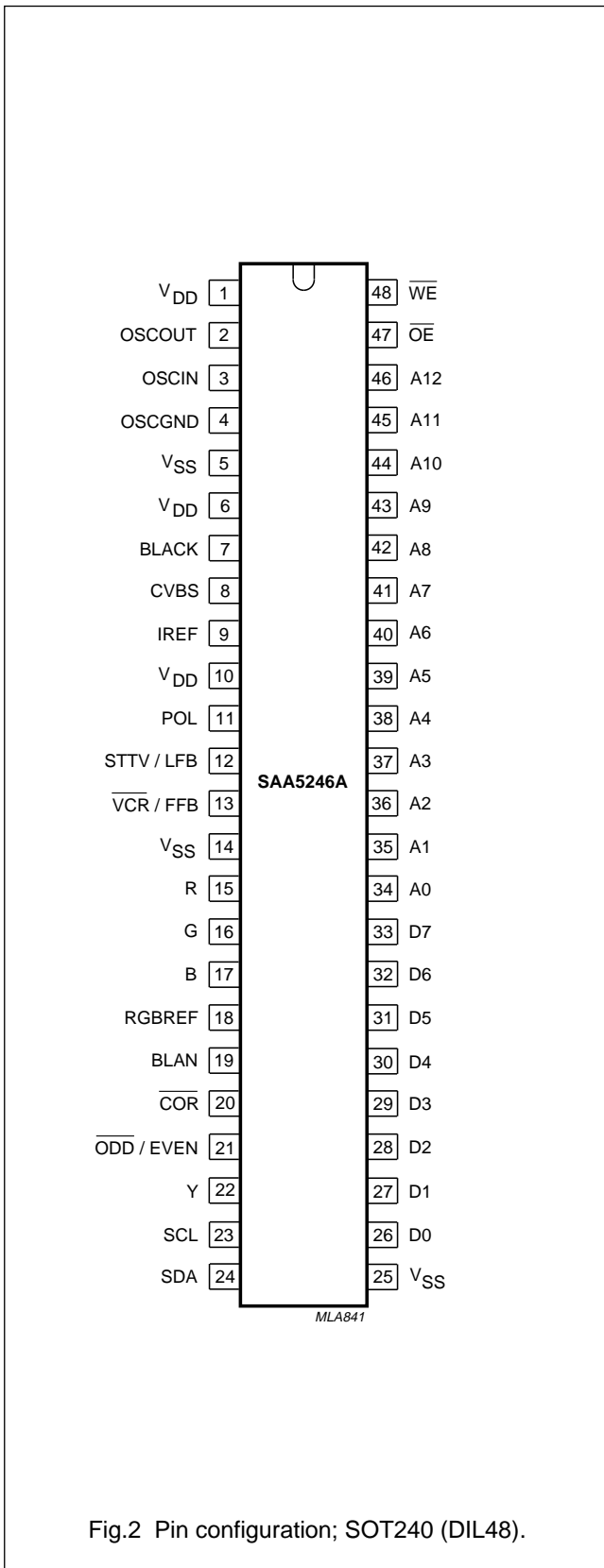


Fig.2 Pin configuration; SOT240 (DIL48).

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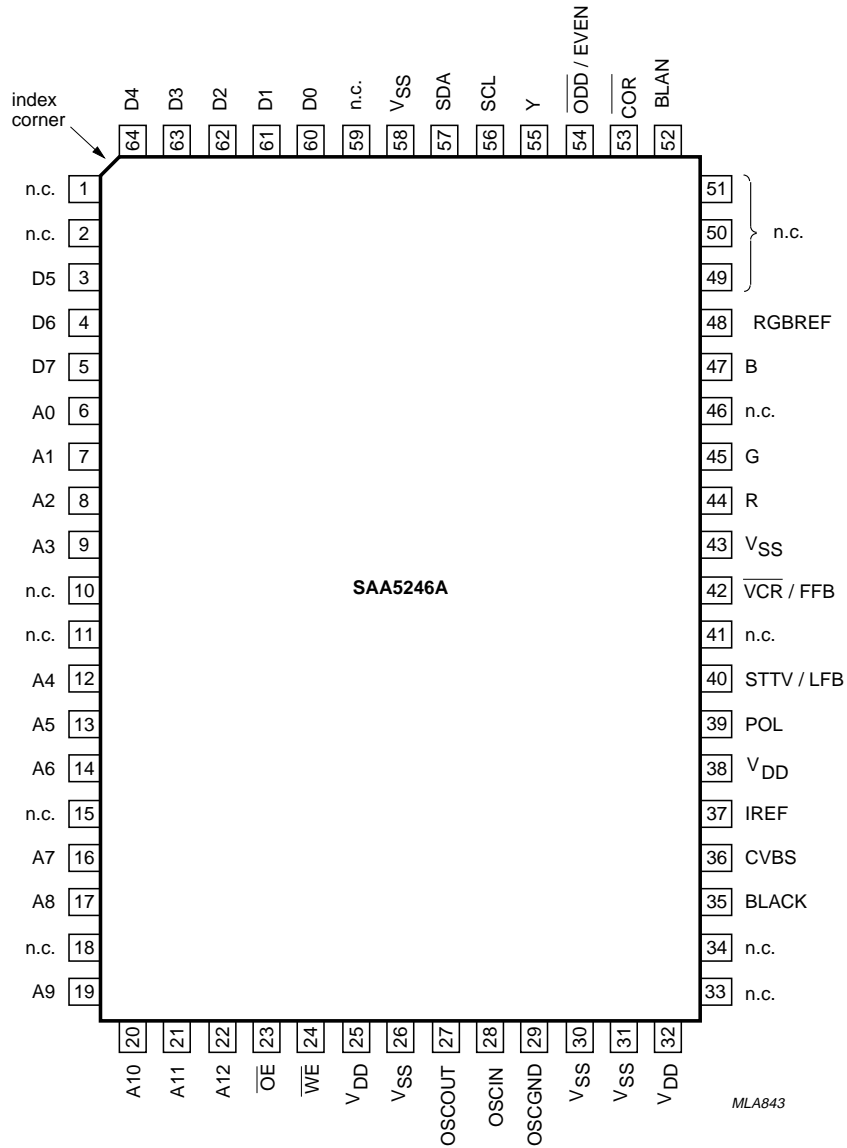


Fig.3 Pin configuration; SOT319 (QFP64).

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**LIMITING VALUES**

In accordance with Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$V_{DD}$	supply voltage (all supplies)	-0.3	6.5	V
$V_I$	input voltage (any input)	-0.3	$V_{DD} + 0.5$	V
$V_O$	output voltage (any output)	-0.3	$V_{DD} + 0.5$	V
$I_O$	output current (each output)	-	$\pm 10$	mA
$I_{IOK}$	DC input or output diode current	-	$\pm 20$	mA
$T_{amb}$	operating ambient temperature	-20	+70	°C
$T_{stg}$	storage temperature	-55	+125	°C
$V_{stat}$	electrostatic handling (see note 1)	-2000	+2000	V

**Note to the Limiting values**

1. Electrostatic handling is equivalent to discharging a 100 pF capacitor through a 1.5 k $\Omega$  series resistor with a 15 ns rise time.

**Failure Rate**

The failure rate at  $T_{amb} = 55$  °C will be a maximum of 1000 FITS (1 FIT =  $1 \times 10^{-9}$  failures per hour).



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**CHARACTERISTICS** $V_{DD} = 5\text{ V} \pm 10\%$ ;  $T_{amb} = -20\text{ to }+70\text{ }^{\circ}\text{C}$ , unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Supplies</b>						
$V_{DD}$	supply voltage range		4.5	5.0	5.5	V
$I_{DD}$	total supply current		–	64	128	mA
<b>Inputs</b>						
<b>CVBS</b>						
$V_{syn}$	sync amplitude		0.1	0.3	0.6	V
$t_{syn}$	delay from CVBS to TCS output from STTV buffer (nominal video, average of leading/trailing edge)		–150	0	+150	ns
$t_{syd}$	change in sync delay between all black and all white video input at nominal levels		0	–	25	ns
$V_{vid(p-p)}$	video input amplitude (peak-to-peak)		0.7	1.0	1.4	V
	display PLL catching range		$\pm 7$	–	–	%
$Z_{src}$	source impedance		–	–	250	$\Omega$
$C_I$	input capacitance		–	–	10	pF
<b>IREF</b>						
$R_g$	resistor to ground		–	27	–	k $\Omega$
<b>POL</b>						
$V_{IL}$	LOW level input voltage		–0.3	–	+0.8	V
$V_{IH}$	HIGH level input voltage		2.0	–	$V_{DD}+0.5$	V
$I_{LI}$	input leakage current	$V_I = 0\text{ to }V_{DD}$	–10	–	+10	$\mu\text{A}$
$C_I$	input capacitance		–	–	10	pF
<b>LFB</b>						
$V_{IL}$	LOW level input voltage		–0.3	–	+0.8	V
$V_{IH}$	HIGH level input voltage		2.0	–	$V_{DD}+0.5$	V
$I_{LI}$	input leakage current	$V_I = 0\text{ to }V_{DD}$	–10	–	+10	$\mu\text{A}$
$I_I$	input current	note 1	–1	–	+1	mA
$t_{LFB}$	delay between LFB front edge and input video line sync		–	250	–	ns
<b>VCR/FFB</b>						
$V_{IL}$	LOW level input voltage		–0.3	–	+0.8	V
$V_{IH}$	HIGH level input voltage		2.0	–	$V_{DD}+0.5$	V
$I_{LI}$	input leakage current	$V_I = 0\text{ to }V_{DD}$	–10	–	+10	$\mu\text{A}$
$I_I$	input current	note 1	–1	–	+1	mA

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>RGBREF</b>						
V <sub>IL</sub>	LOW level input voltage		-0.3	-	V <sub>DD</sub> +0.5	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = 0 to V <sub>DD</sub>	-10	-	+10	μA
I <sub>DC</sub>	DC current		-	-	10	mA
<b>SCL</b>						
V <sub>IL</sub>	LOW level input voltage		-0.3	-	+1.5	V
V <sub>IH</sub>	HIGH level input voltage		3.0	-	V <sub>DD</sub> +0.5	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = 0 to V <sub>DD</sub>	-10	-	+10	μA
f <sub>SCL</sub>	clock frequency		0	-	100	kHz
t <sub>r</sub>	input rise time	10% to 90%	-	-	2	μs
t <sub>f</sub>	input fall time	90% to 10%	-	-	2	μs
C <sub>I</sub>	input capacitance		-	-	10	pF
<b>Inputs/outputs</b>						
<b>CRYSTAL OSCILLATOR (OSCIN; OSCOUT)</b>						
f <sub>X TAL</sub>	crystal frequency		-	27	-	MHz
V <sub>OSC</sub>	oscillation amplitude (peak-to-peak value)		-	1.5	-	V
G <sub>v</sub>	small signal voltage gain		-	1	-	V/V
G <sub>m</sub>	mutual conductance		5	-	-	mA/V
C <sub>I</sub>	input capacitance		-	-	10	pF
C <sub>FB</sub>	feedback capacitance		-	1	-	pF
<b>BLACK</b>						
C <sub>blk</sub>	storage capacitor to ground		-	100	-	nF
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = 0 to V <sub>DD</sub>	-10	-	+10	μA
<b>SDA</b>						
V <sub>IL</sub>	LOW level input voltage		-0.3	-	+1.5	V
V <sub>IH</sub>	HIGH level input voltage		3.0	-	V <sub>DD</sub> +0.5	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = 0 to V <sub>DD</sub>	-10	-	+10	μA
C <sub>I</sub>	input capacitance		-	-	10	pF
t <sub>r</sub>	input rise time	10% to 90%	-	-	2	μs
t <sub>f</sub>	input fall time	90% to 10%	-	-	2	μs
V <sub>OL</sub>	LOW level output voltage	I <sub>OL</sub> = 3 mA	0	-	0.5	V
t <sub>f</sub>	output fall time	3 V to 1 V	-	-	200	ns
C <sub>L</sub>	load capacitance		-	-	400	pF

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>D0 TO D7</b>						
V <sub>IL</sub>	LOW level input voltage		-0.3	-	+0.8	V
V <sub>IH</sub>	HIGH level input voltage		2.0	-	V <sub>DD</sub> +0.5	V
I <sub>LI</sub>	input leakage current		-10	-	+10	μA
C <sub>I</sub>	input capacitance		-	-	10	pF
V <sub>OL</sub>	LOW level output voltage	I <sub>OL</sub> = +1.6 mA	0	-	0.4	V
V <sub>OH</sub>	HIGH level output voltage	I <sub>OH</sub> = -0.2 mA	2.4	-	V <sub>DD</sub>	V
t <sub>r</sub>	output rise time	0.6 V to 2.2 V	-	-	50	ns
t <sub>f</sub>	output fall time	2.2 V to 0.6 V	-	-	50	ns
C <sub>L</sub>	load capacitance		-	-	120	pF
<b>Outputs</b>						
<b>STTV</b>						
G <sub>stt</sub>	gain of STTV relative to video input		0.9	1.0	1.1	
V <sub>tcs</sub>	TCS amplitude		0.2	0.3	0.45	V
V <sub>DCs</sub>	DC shift between TCS output and nominal video output		-	-	0.15	V
I <sub>O</sub>	output drive current		-	-	3.0	mA
C <sub>L</sub>	load capacitance		-	-	100	pF
<b>A0 TO A12 ADDRESS OUTPUT TO MEMORY</b>						
V <sub>OL</sub>	LOW level output voltage	I <sub>OL</sub> = +1.6 mA	0	-	0.4	V
V <sub>OH</sub>	HIGH level output voltage	I <sub>OH</sub> = -0.2 mA	2.4	-	V <sub>DD</sub>	V
C <sub>L</sub>	load capacitance		-	-	120	pF
t <sub>r</sub>	output rise time	0.6 V to 2.2 V	-	-	50	ns
t <sub>f</sub>	output fall time	2.2 V to 0.6 V	-	-	50	ns
<b>OE, WE</b>						
V <sub>OL</sub>	LOW level output voltage	I <sub>OL</sub> = +1.6 mA	0	-	0.4	V
V <sub>OH</sub>	HIGH level output voltage	I <sub>OH</sub> = -0.2 mA	2.4	-	V <sub>DD</sub>	V
C <sub>L</sub>	load capacitance		-	-	120	pF
t <sub>r</sub>	output rise time	0.6 V to 2.2 V	-	-	50	ns
t <sub>f</sub>	output fall time	2.2 V to 0.6 V	-	-	50	ns

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>R, G AND B</b>						
$V_{OL}$	LOW level output voltage	$I_{OL} = 2 \text{ mA}$	0	–	0.2	V
$V_{OH}$	HIGH level output voltage	$I_{OH} = -1.6 \text{ mA}$ ; $RGBREF \leq V_{DD} - 2 \text{ V}$ ; note 2	$RGBREF - 0.25 \text{ V}$	$RGBREF$	$RGBREF + 0.25 \text{ V}$	V
$I_{DC}$	DC current		–	–	-3.3	mA
$ Z_o $	output impedance		–	–	200	$\Omega$
$C_L$	load capacitance		–	–	50	pF
$t_r$	output rise time	10% to 90%	–	–	20	ns
$t_f$	output fall time	90% to 10%	–	–	20	ns
<b>BLAN</b>						
$V_{OL}$	LOW level output voltage	$I_{OL} = 0.2 \text{ mA}$	0	–	0.4	V
$V_{OH}$	HIGH level output voltage	$I_{OH} = -0.2 \text{ mA}$ ; $V_{DD} = 4.5 \text{ V}$ ; note 2	1.1	–	–	V
$V_{OH}$	HIGH level output voltage	$I_{OH} = 0 \text{ mA}$ ; $V_{DD} = 5.5 \text{ V}$ ; note 2	–	–	2.8	V
$C_L$	load capacitance		–	–	50	pF
$t_r$	output rise time	10% to 90%	–	–	20	ns
$t_f$	output fall time	90% to 10%	–	–	20	ns
<b>ODD/EVEN</b>						
$V_{OL}$	LOW level output voltage	$I_{OL} = +1.6 \text{ mA}$	0	–	0.4	V
$V_{OH}$	HIGH level output voltage	$I_{OH} = -1.6 \text{ mA}$	$V_{DD} - 0.4$	–	$V_{DD}$	V
$C_L$	load capacitance		–	–	120	pF
$t_r$	output rise time	0.6 to 2.2 V	–	–	50	ns
$t_f$	output fall time	2.2 to 0.6 V	–	–	50	ns
<b>COR AND Y (OPEN DRAIN)</b>						
$V_{OH}$	pull-up voltage at pin		–	–	$V_{DD}$	V
$V_{OL}$	LOW level output voltage	$I_{OL} = +2 \text{ mA}$	0	–	0.4	V
$V_{OL}$	LOW level output voltage	$I_{OL} = +5 \text{ mA}$	0	–	1.0	V
$C_L$	load capacitance		–	–	25	pF
$t_f$	output fall time	load resistor of 1.2 k $\Omega$ to $V_{DD}$ ; measured between $V_{DD} - 0.5$ and 1.5 V	–	–	50	ns
$I_{LO}$	output leakage current	$V_I = 0$ to $V_{DD}$	-10	–	+10	$\mu\text{A}$
$T_{SK}$	skew delay between display outputs R, G, B, COR, Y and BLAN		–	–	20	ns

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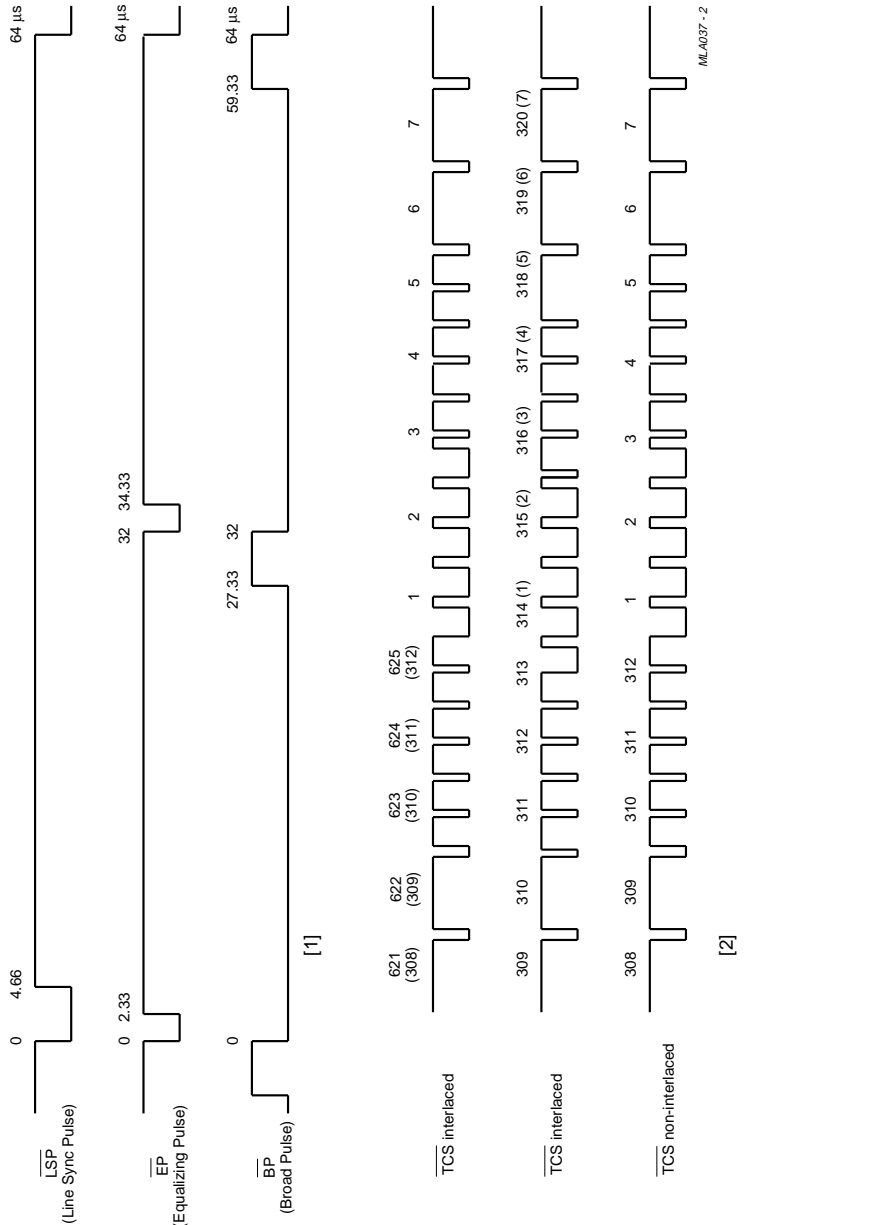
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Timing</b>						
MEMORY INTERFACE						
t <sub>CY</sub>	cycle time		–	500	–	ns
t <sub>OE</sub>	address change to $\overline{OE}$ LOW		55	–	–	ns
t <sub>ADDR</sub>	address active time		450	500	–	ns
t <sub>roEW</sub>	$\overline{OE}$ pulse width read		295	–	–	ns
t <sub>wOEW</sub>	$\overline{OE}$ pulse width write		100	–	–	ns
t <sub>ACC</sub>	access time from address data valid		–	–	150	ns
t <sub>DH</sub>	data hold time from $\overline{OE}$ HIGH or address change		0	–	150	ns
t <sub>WEW</sub>	$\overline{WE}$ pulse width		100	–	–	ns
t <sub>DS</sub>	data set-up time to $\overline{WE}$ HIGH		60	–	–	ns
t <sub>DHWE</sub>	data hold time from $\overline{WE}$ HIGH		20	–	–	ns
t <sub>WR</sub>	write recovery time		20	–	–	ns
t <sub>DE</sub>	data enable from $\overline{WE}$ LOW		60	–	–	ns
I <sup>2</sup> C-BUS						
t <sub>LOW</sub>	clock LOW period		4	–	–	μs
t <sub>HIGH</sub>	clock HIGH period		4	–	–	μs
t <sub>SU;DAT</sub>	data set-up time		250	–	–	ns
t <sub>HD;DAT</sub>	data hold time		170	–	–	ns
t <sub>SU;STO</sub>	set-up time from clock HIGH to STOP		4	–	–	μs
t <sub>BUF</sub>	START set-up time following a STOP		4	–	–	μs
t <sub>HD;STA</sub>	START hold time		4	–	–	μs
t <sub>SU;STA</sub>	START set-up time following clock LOW-to-HIGH transition		4	–	–	μs

**Notes to the characteristics**

1. This current is the maximum allowed into the inputs when line and field flyback signals are connected to these inputs. Series current limiting resistors must be used to limit the input currents to  $\pm 1$  mA.
2. Can be pulled higher by external pull-up resistor, (maximum leakage current  $\approx 200$  μA).

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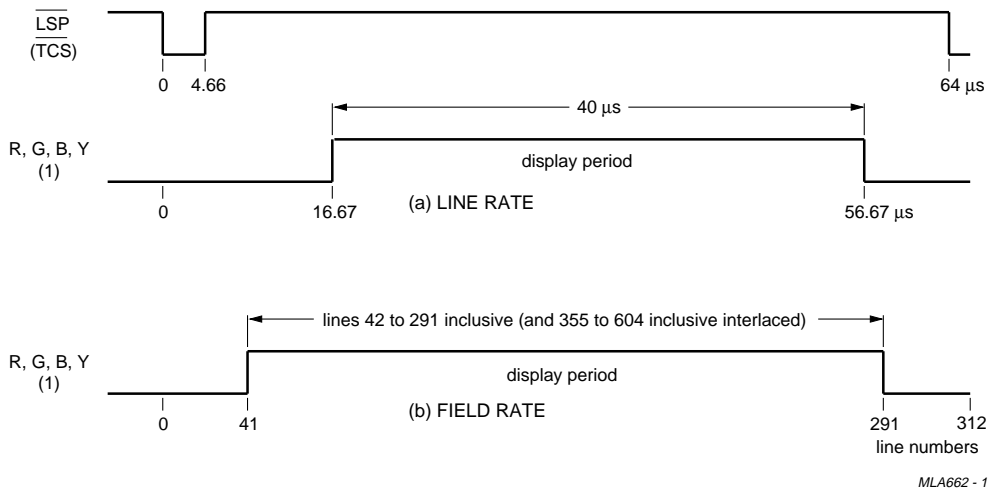


TCS is available on STTV/LFB pin.  
 [1]  $\overline{\text{LSP}}$ ,  $\overline{\text{EP}}$  and  $\overline{\text{BP}}$  are combined to give  $\overline{\text{TCS}}$  as shown below. All timings measured from falling edge of  $\overline{\text{LSP}}$ .  
 [2] Line numbers placed in the middle of the line. Equivalent count numbers in brackets.

Fig.4 Composite sync waveforms.

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(1) also BLAN in character and box blanking

Fig.5 Display output timing (a) line rate (b) field rate.

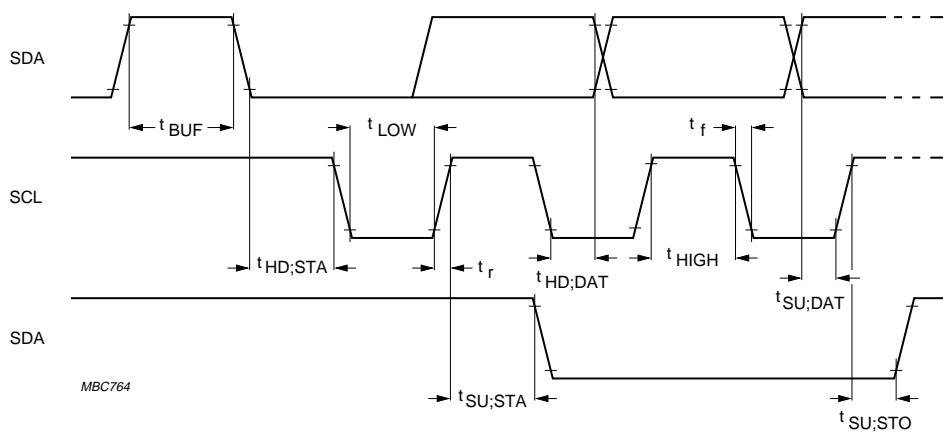
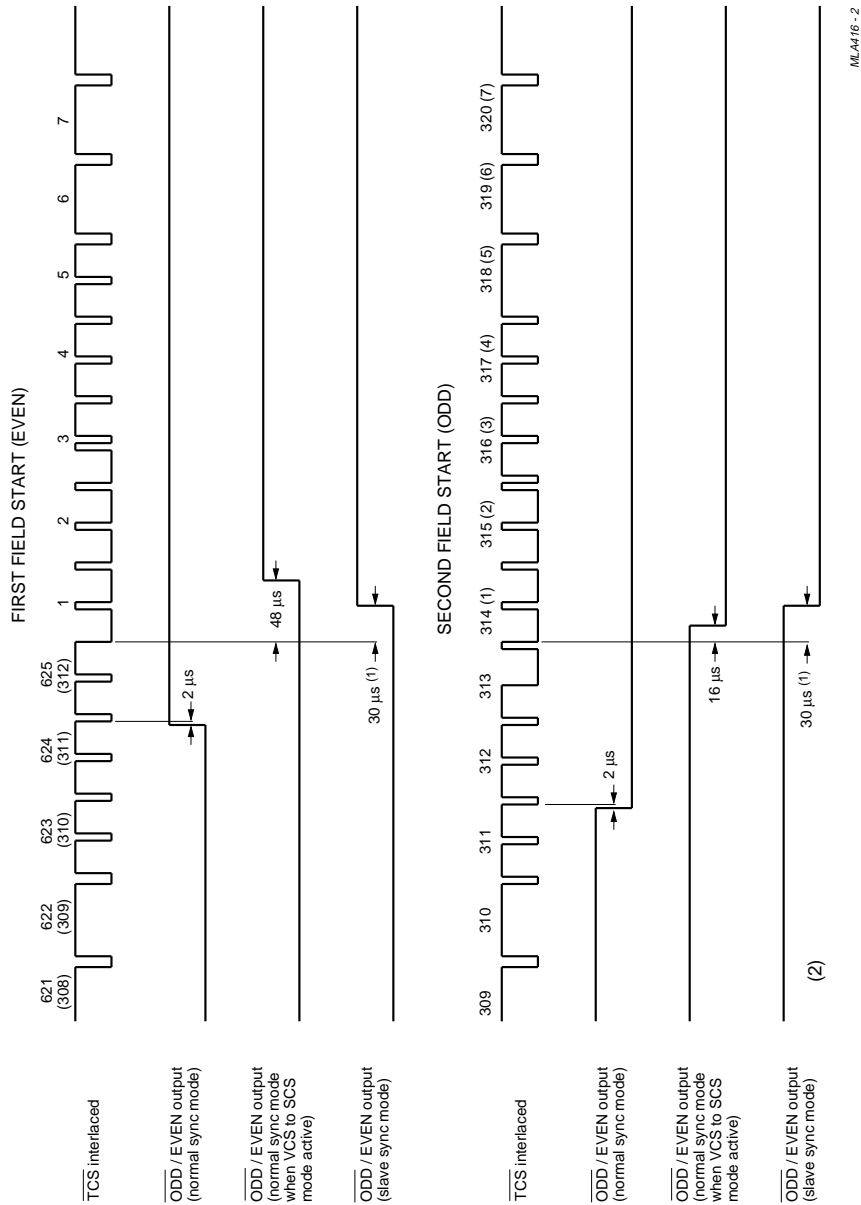


Fig.6 I<sup>2</sup>C-bus timing.

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MLA416 - 2

(1) or 62 μs if R1 D2.D1.D0 = 111.

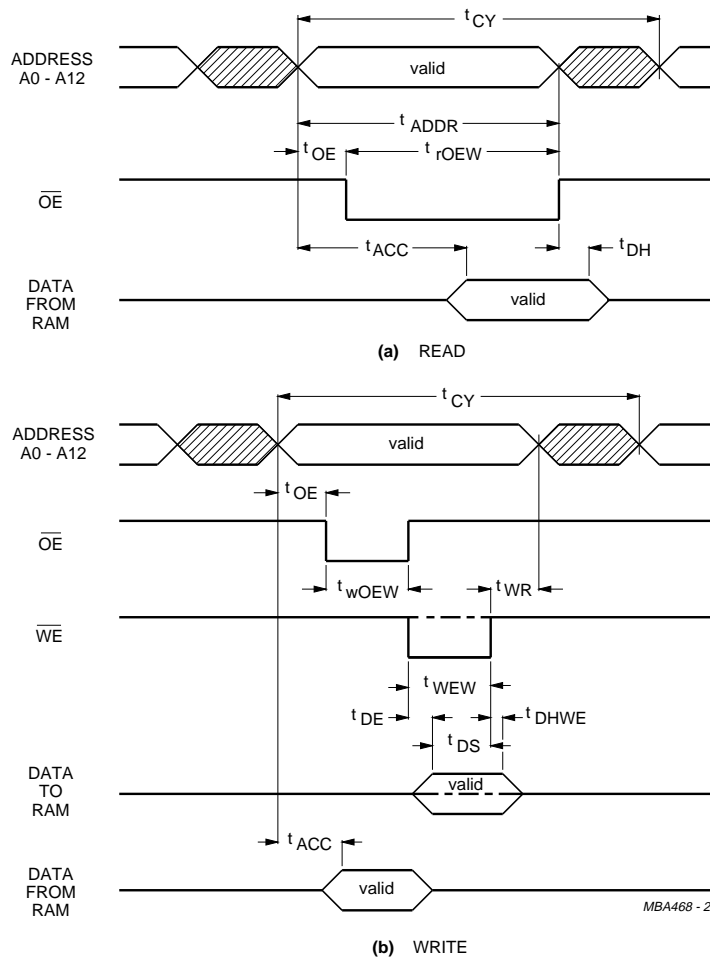
(2) Line numbers placed in the middle of the line. Equivalent count numbers in brackets.

Fig.7 ODD/EVEN timing.



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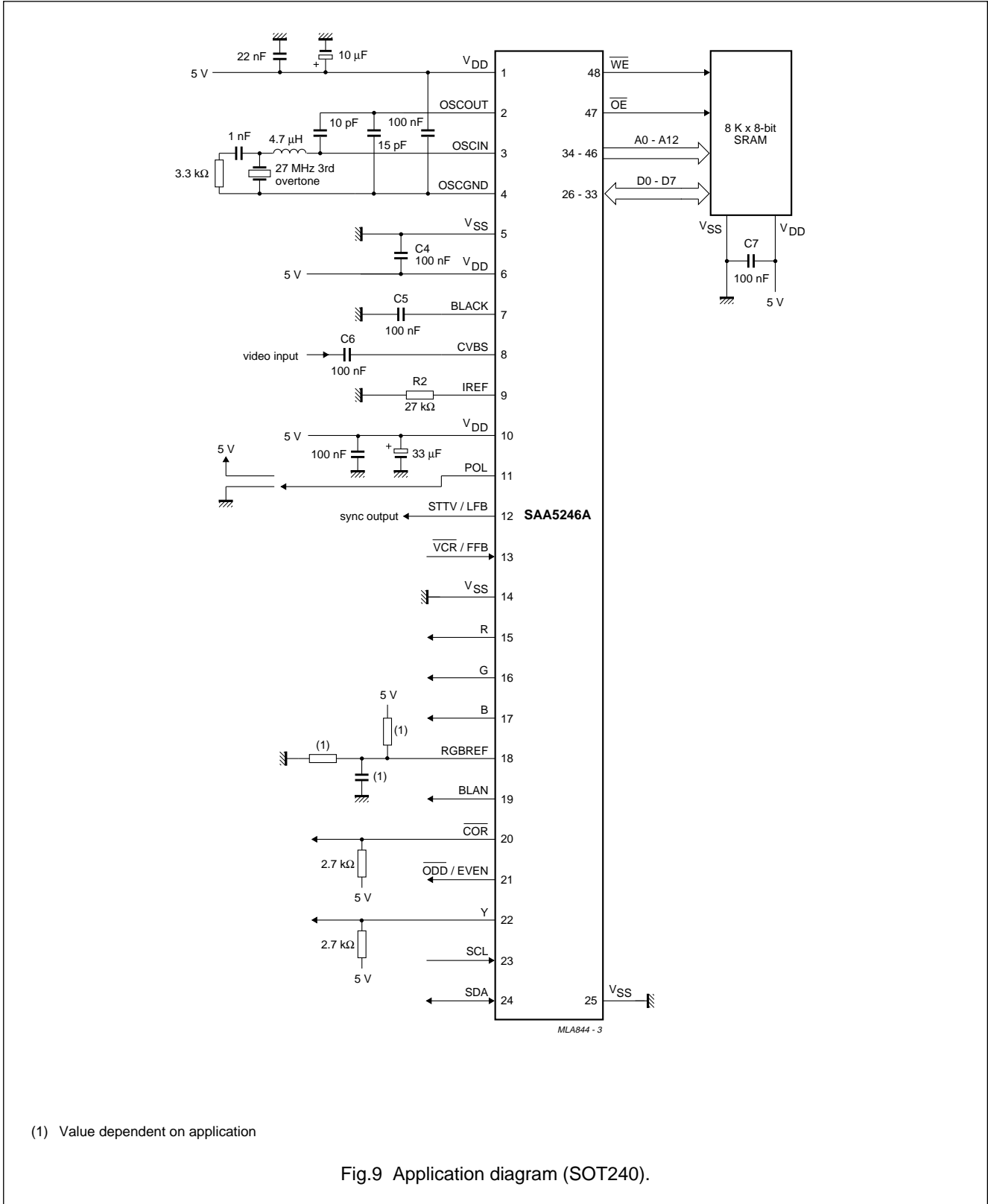
----- Level during flicker stopped cycle.

Fig.8 Memory interface timing (a) read (b) write.

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APPLICATION INFORMATION



(1) Value dependent on application

Fig.9 Application diagram (SOT240).

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**SAA5246A page memory organization**

The organization of the page memory is illustrated by Fig.10. The SAA5246A provides an additional row as compared with first generation decoders; this brings the display format up to 40 characters by 25 rows. Rows 0 to 23 form the teletext page; row 24 is the extra row available for software generated status messages and FLOF/FASTEXT prompt information.

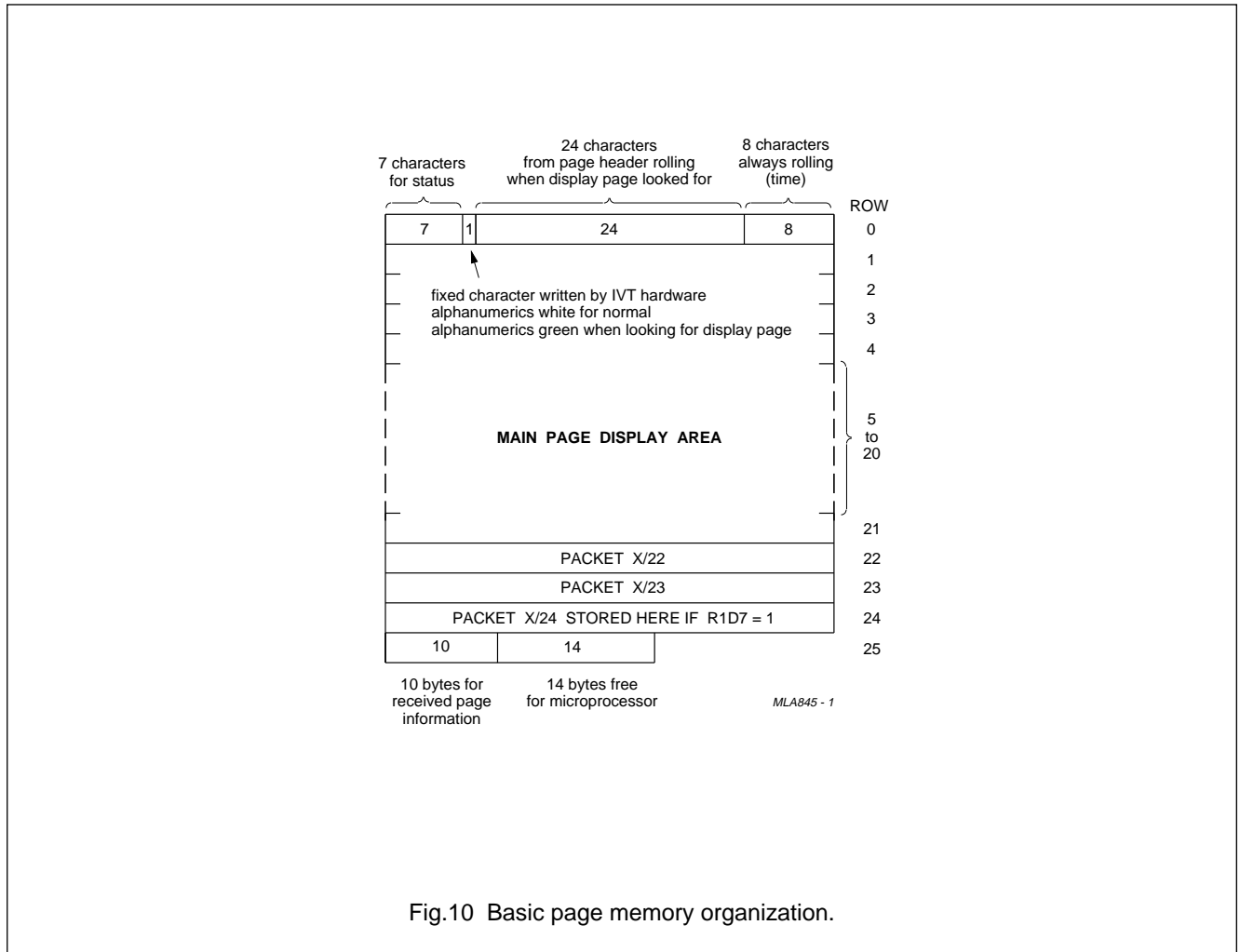


Fig.10 Basic page memory organization.

**Note to Fig.10**

Row 0

Row 0 is for the page header. The first seven columns (0 to 6) are free for status messages. The eighth is an alphanumeric white or green control character, written automatically by SAA5246A to give a green rolling header when a page is being looked for. The last eight characters are for rolling time.

Row 25

The first 10 bytes of Row 25 contain control data relating to the received page as shown in Table 1. The remaining 14 bytes are free for use by the microprocessor.

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**Table 1** Row 25 received control data format.

D0	PU0	PT0	MU0	MT0	HU0	HT0	C7	C11	MAG0	0
D1	PU1	PT1	MU1	MT1	HU1	HT1	C8	C12	MAG1	0
D2	PU2	PT2	MU2	MT2	HU2	C5	C9	C13	MAG2	0
D3	PU3	PT3	MU3	C4	HU3	C6	C10	C14	0	0
D4	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	FOUND	0
D5	0	0	0	0	0	0	0	0	0	PBLF
D6	0	0	0	0	0	0	0	0	0	0
D7	0	0	0	0	0	0	0	0	0	0
Column	0	1	2	3	4	5	6	7	8	9

**Where:**

Page number

MAG magazine

PU page units

PT page tens

PBLF page being looked for

FOUND LOW for page has been found

HAM.ER Hamming error in corresponding byte

Page sub-code

MU minutes units

MT minutes tens

HU hours units

HT hours tens

C4-C14 transmitted control bits.

When in extension packet enabled mode the rows of information are organized as illustrated by Fig.11.

Row 23 of the extension page, as shown in Fig.11, contains packet 8/30. Packet 8/30 is mapped into the SAA5246A memory as follows:

8/30/0 and 8/30/1 to Chapter 4 Row 23

8/30/2 and 8/30/3 to Chapter 5 Row 23

8/30/4 to 8/30/15 to Chapter 6 Row 23



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## Register maps

SAA5246A mode registers R0 to R11 are shown in Table 2. R0 to R10 are WRITE only; R11 is READ/WRITE; R11B is READ only. Register map (R3), for page requests, is shown in detail in Table 4.

Table 2 Register map.

REGISTER		D7	D6	D5	D4	D3	D2	D1	D0
Adv. control	0	X24 POS	FREE RUN PLL	AUTO ODD/EVEN	DISABLE HDR ROLL	–	DISABLE ODD/EVEN	VCR MODE	R11/R11B SELECT
Mode	1	VCS TO SCS	7 + P/8-BIT	ACQ ON/OFF	EXT. PACKET ENABLE	DEW/FULL FIELD	TCS ON FFB MODE	T1	T0
Page request address	2	HAM. CHECK	BANK SELECT A2	ACQ CIRCUIT A1	ACQ CIRCUIT A0	TB	START COLUMN SC2	START COLUMN SC1	START COLUMN SC0
Page request data	3	–	–	–	PRD4	PRD3	PRD2	PRD1	PRD0
Display chapter	4	–	–	–	–	–	A2	A1	A0
Display control (normal)	5	BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN
Display control (newsflash /subtitle)	6	BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN
Display mode	7	STATUS TOP	CURSOR ON	REVEAL ON	BOTTOM HALF	DOUBLE HEIGHT	BOX ON 24	BOX ON 1-23	BOX ON 0
Active chapter	8	–	–	–	–	CLEAR MEM.	A2	A1	A0
Cursor row	9	–	–	–	R4	R3	R2	R1	R0
Cursor column	10	–	–	C5	C4	C3	C2	C1	C0
Cursor data	11	D7	D6	D5	D4	D3	D2	D1	D0
Device status	11B	625/525 SYNC	ROM VER R4	ROM VER R3	ROM VER R2	ROM VER R1	ROM VER R0	DATA QUALITY	VCS SIGNAL QUALITY

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### Notes to Table 2

1. '–' indicates a bit which does not exist and must be written to logic 0 for future compatibility.
2. All bits in registers R0 to R10 are cleared to logic 0 on power-up except bits D0 and D1 of registers R1, R5 and R6 which are set to logic 1.
3. All memory is cleared to 'space' (00100000) on power-up, except Row 0 Column 7 Chapter 0, which is 'alpha' white (00000111) as the acquisition circuit is enabled but the page is on hold.
4. TB must be set to logic 0 for normal operation.
5. The I<sup>2</sup>C-bus slave address is 0010001.

### Register description

#### R0 ADVANCED CONTROL - auto increments to Register 1

R11/R11B SELECT	Selects reading of R11 or R11B
VCR MODE	Selects short time constant of PLL when logic 1
DISABLE $\overline{\text{ODD}}/\text{EVEN}$	Forces $\overline{\text{ODD}}/\text{EVEN}$ output LOW when logic 1
DISABLE HDR ROLL	Disables green rolling header and time
AUTO $\overline{\text{ODD}}/\text{EVEN}$	When set forces $\overline{\text{ODD}}/\text{EVEN}$ low if any TV picture displayed, if DISABLE $\overline{\text{ODD}}/\text{EVEN}$ = 0
FREE RUN PLL	Will force the PLL to free run in all conditions
X24 POS	Automatic display of FASTEXT prompt row when logic 1

#### R1 MODE - auto increments to Register 2

T0, T1	Interlace/non-interlace 312/313 line control (see Table 4)
TCS ON FFB MODE	Text composite sync or direct sync select (see Table 4 for FFB mode selection)
$\overline{\text{DEW}}/\text{FULL FIELD}$	Field-flyback or full channel mode
EXT. PACKET ENABLE	Allocates 2K bytes memory per chapter
ACQ $\overline{\text{ON}}/\text{OFF}$	Acquisition circuits turned off when logic 1
$\overline{7+P}/8\text{-BIT}$	7 bits with parity checking or 8-bit mode
VCS TO SCS	When logic 1 enables display of messages with 60 Hz input signal

#### R2 PAGE REQUEST ADDRESS - auto increments to Register 3

HAM.CHECK	When logic 1 enables Hamming 8/4 checking of extension packet 27/0, 27/1 and 8/30/x
COL SC0 - SC2	Point to start column for page request data (see Table 3)
TB	Must be logic 0 for normal operation
ACQ CIRCUIT	Selects one of four acquisition circuits
BANK SELECT	Selects which bank of four chapters is being accessed, when EXT. PACKET ENABLE = 0

#### R3 PAGE REQUEST DATA - does not auto increment (see Table 3)

#### R4 DISPLAY CHAPTER - auto increments to Register 5

determines which of the 8 pages is displayed

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**R5 NORMAL DISPLAY CONTROL - auto increments to Register 6**

PON	Picture on
TEXT	Text on
COR	Contrast reduction on
BKGND	Background colour on

These functions have IN and OUT referring to inside and outside the boxing function respectively.

**R6 NEWSFLASH DISPLAY - auto increments to Register 7**

PON	Picture on
TEXT	Text on
COR	Contrast reduction on
BKGND	Background colour on

These functions have IN and OUT referring to inside and outside the boxing function respectively.

**R7 DISPLAY MODE - does not auto increment**

BOX ON 0	Boxing function allowed on Row 0
BOX ON 1-23	Boxing function allowed on Row 1-23
BOX ON 24	Boxing function allowed on Row 24
DOUBLE HEIGHT	To display double height text
BOTTOM HALF	To select bottom half of page when DOUBLE HEIGHT = 1
REVEAL ON	To reveal concealed text
CURSOR ON	To display cursor
STATUS TOP	Row 25 displayed above or below the main text

**R8 ACTIVE CHAPTER - auto increments to Register 9**

A0 to A2	Active chapter
CLEAR MEMORY	When set to 1, clears the display memory. This bit is automatically reset

**R9 CURSOR ROW - auto increments to Register 10**

R0 to R4	Active row for data written to or read from memory via the I <sup>2</sup> C-bus
----------	---

**R10 CURSOR COLUMN - auto increments to Register 11 or 11B**

C0 to C5	Active column for data written to or read from memory via the I <sup>2</sup> C-bus
----------	--

**R11 CURSOR DATA - does not auto increment**

D0 to D7	Data read from/written to memory via I <sup>2</sup> C, at location pointed to by R8, R9 and R10. This location automatically increments each time R11 is accessed
----------	--

**R11B DEVICE STATUS - does not auto increment**

VCS SIGNAL QUALITY	Indicates that the video signal quality is good and PLL is phase locked to input video when = 1
DATA QUALITY	If good Teletext data is detected then = 1
ROM VER R0 to R4	Indicated language/ROM variant. See Table 6 - Table 13.
$\overline{625/525}$ SYNC	If the input video is a 525 line signal when = 1



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**Table 3** Register map for page requests (R3).

START COLUMN	PRD4	PRD3	PRD2	PRD1	PRD0
0	Do care Magazine	$\overline{\text{HOLD}}$	MAG2	MAG1	MAG0
1	Do care Page tens	PT3	PT2	PT1	PT0
2	Do care Page units	PU3	PU2	PU1	PU0
3	Do care Hours tens	X	X	HT1	HT0
4	Do care Hours units	HU3	HU2	HU1	HU0
5	Do care Minutes tens	X	MT2	MT1	MT0
6	Do care Minutes units	MU3	MU2	MU1	MU0

**Notes to Table 3**

- Abbreviations are as for Table 1 except for DO CARE bits.
- When the DO CARE bit is set to logic 1 this means the corresponding digit is to be taken into account for page request. If the DO CARE bit is set to logic 0 the digit is ignored. This allows, for example, 'normal' or 'timed page' selection.
- If  $\overline{\text{HOLD}}$  is set LOW, the page is held and not updated
- Columns auto-increment on successive I<sup>2</sup>C-bus transmission bytes
- 'X' = Don't care

**Table 4** Interlace/non-interlace 312/313 line control and ODD/EVEN field detection option

TCS ON FFB MODE	T1	T0	RESULT
x	0	0	interlaced 312.5/312.5 lines
x	0	1	non-interlaced 312/313 lines (note 1)
x	1	0	non-interlaced 312/312 lines (note 1)
0	1	1	SCS (scan composite sync) mode: FFB leading edge in first broad pulse of field M7 version onwards
1	1	1	SCS (scan composite sync) mode: FFB leading edge in second broad pulse of field M7 version onwards

**Notes to Table 4**

- Reverts to interlaced mode if a newflash or subtitle is being displayed.
- 'x' = Don't care.

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CLOCK SYSTEMS

Crystal oscillator

The oscillator is a low amplitude, low distortion design operation at 27 MHz. It is capable of oscillating with both fundamental and third overtone mode crystals. External components should be used to suppress the fundamental output of the third overtone as illustrated in Fig.12.

Table 5 Crystal characteristics.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
<b>Crystal (27 MHz, 3rd overtone)</b>					
C1	series capacitance	–	1.7	-	pF
C0	parallel capacitance	–	5.2	–	pF
C <sub>L</sub>	load capacitance	–	20	–	pF
R <sub>r</sub>	resonant resistance	–	–	50	Ω
R1	series resistance	–	20	–	Ω
X <sub>a</sub>	ageing	–	–	±5	10 <sup>-6</sup> /yr
X <sub>j</sub>	adjustment tolerance	–	–	±25	10 <sup>-6</sup>
X <sub>d</sub>	drift	–	–	±25	10 <sup>-6</sup>

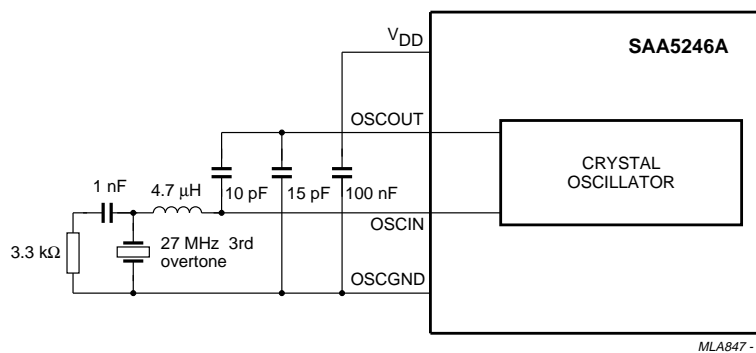


Fig.12 Crystal oscillator application diagram.

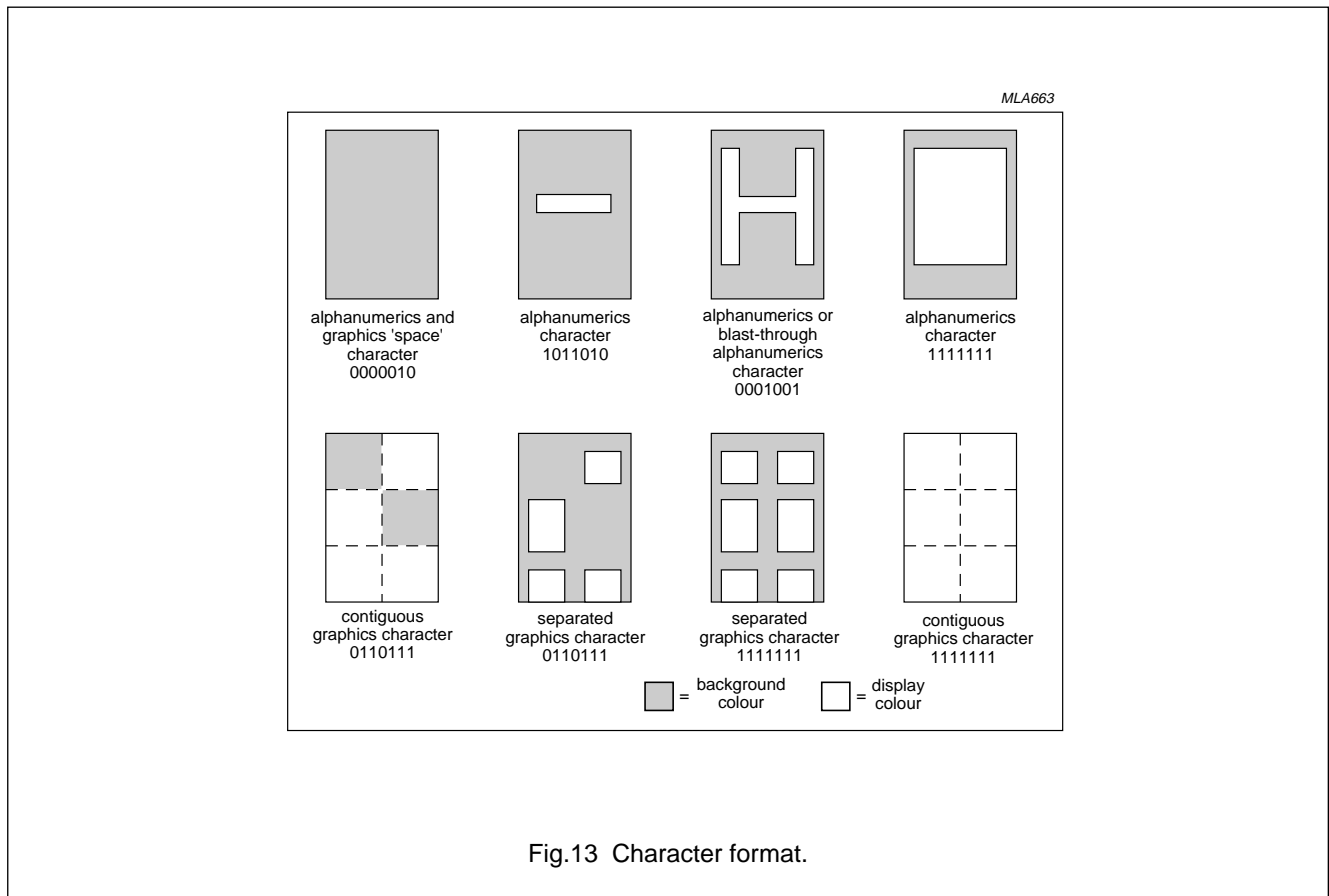
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**Character sets**

The WST specification allows the selection of national character sets via the page header transmission bits, C12 to C14. The basic 96 character sets differ only in 13 national option characters as indicated in Tables 15 - 23 with reference to their table position in the basic character matrix illustrated in Table 14. The SAA5246A automatically decodes transmission bits C12 to C14. Tables 6 - 13 illustrate the character matrices.

Character bytes are listed as transmitted from b1 to b7.





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Table 7 SAA5246AP/H character data input decoding, East European languages

BITS	b <sub>8</sub> →				b <sub>7</sub> →				b <sub>6</sub> →				b <sub>5</sub> →				b <sub>4</sub> b <sub>3</sub> b <sub>2</sub> b <sub>1</sub>			
	0	0	0 or 1	0	0	0	0 or 1	0	0	0	1	1	0	0	1	1	1	1	1	1
row	column	0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15	
0 0 0 0	0	alpha - numerics black	graphics black			0	.	I	P	t	.	p	.	S	É	č	ř	Č	Ú	
0 0 0 1	1	alpha - numerics red	graphics red	!	□	1	□	A	Q	a	□	q	□	°	é	é	ř	č	ď	
0 0 1 0	2	alpha - numerics green	graphics green	"	□	2	□	B	R	b	□	r	□	ä	ä	á	ž	č	Ď	
0 0 1 1	3	alpha - numerics yellow	graphics yellow	#	□	3	□	C	S	c	□	s	□	ö	ö	ē	ř	ž	Ī	
0 1 0 0	4	alpha - numerics blue	graphics blue	X	□	4	□	D	T	d	□	t	□	\$	X	č	ň	½	Ĺ	
0 1 0 1	5	alpha - numerics magenta	graphics magenta	%	□	5	□	E	U	e	□	u	□	€	€	Á	ó	ó	Ī	
0 1 1 0	6	alpha - numerics cyan	graphics cyan	&	□	6	□	F	V	f	□	v	□	⊗	⊗	É	ó	ó	Ĺ	
0 1 1 1	7	alpha - numerics white <sup>(2)</sup>	graphics white	'	□	7	□	G	W	g	□	w	□	?	?	í	ú	ú	N	
1 0 0 0	8	flash	conceal display	(	□	8	□	H	X	h	□	x	□	ö	ö	ē	š	ž	ň	
1 0 0 1	9	steady <sup>(2)</sup>	contiguous graphics <sup>(2)</sup>	)	□	9	□	I	Y	i	□	y	□	ü	ä	ú	ž	đ	Ñ	
1 0 1 0	10	end box <sup>(2)</sup>	separated graphics	*	□	:	□	J	Z	j	□	z	□	β	ü	š	ž	š	ř	
1 0 1 1	11	start box	ESC <sup>(1)</sup>	+	□	;	□	K	Ā	k	□	ā	□	Ā	Ā	č	ž	č	Ř	
1 1 0 0	12	normal height <sup>(2)</sup>	black back - ground <sup>(2)</sup>	,	□	<	□	L	Š	l	□	š	□	ö	ö	ž	š	ž	Ř	
1 1 0 1	13	double height	new back - ground	-	□	=	□	M	Ā	m	□	ā	□	ü	ā	ý	ž	đ	ř	
1 1 1 0	14	SQ <sup>(1)</sup>	hold graphics	.	□	>	□	N	Ī	n	□	ī	□	^	ü	í	č	š	Y	
1 1 1 1	15	SI <sup>(1)</sup>	release graphics <sup>(2)</sup>	/	□	?	□	O	i	o	□	□	□	□	□	ř	ó	ē	Ē	

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Notes for character version number (00001) see Register 11B

1. These control characters are reserved for compatibility with other data codes.
2. These control characters are presumed before each row begins.









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**Table 11** SAA5246AP/L character data input decoding, Arabic and Hebrew languages.

BITS	b <sub>8</sub> →				b <sub>7</sub> →				b <sub>6</sub> →				b <sub>5</sub> →				b <sub>4</sub> b <sub>3</sub> b <sub>2</sub> b <sub>1</sub>			
	0	0	0 or 1	0	0 or 1	0	0	0	0	0	0	0	0 or 1	0	0 or 1	1	1	1	1	1
row	column	0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15	
0 0 0 0	0	alpha - numerics black	graphics black	□	□	0	□	@	P	N	□	J	□	ع	ا	ا	ا	ا	ا	
0 0 0 1	1	alpha - numerics red	graphics red	!	□	1	□	A	Q	I	□	□	□	ع	ا	ا	ا	ا	ا	
0 0 1 0	2	alpha - numerics green	graphics green	"	□	2	□	B	R	ا	□	□	□	ا	ا	ا	ا	ا	ا	
0 0 1 1	3	alpha - numerics yellow	graphics yellow	£	□	3	□	C	S	T	□	□	□	ا	ا	ا	ا	ا	ا	
0 1 0 0	4	alpha - numerics blue	graphics blue	\$	□	4	□	D	T	ا	□	□	□	ا	ا	ا	ا	ا	ا	
0 1 0 1	5	alpha - numerics magenta	graphics magenta	%	□	5	□	E	U	I	□	□	□	ا	ا	ا	ا	ا	ا	
0 1 1 0	6	alpha - numerics cyan	graphics cyan	&	□	6	□	F	V	I	□	□	□	ا	ا	ا	ا	ا	ا	
0 1 1 1	7	alpha - numerics white <sup>(2)</sup>	graphics white	'	□	7	□	G	W	ا	□	□	□	ا	ا	ا	ا	ا	ا	
1 0 0 0	8	flash	conceal display	(	□	8	□	H	X	ا	□	□	□	)	ا	ا	ا	ا	ا	
1 0 0 1	9	steady <sup>(2)</sup>	contiguous graphics <sup>(2)</sup>	)	□	9	□	I	Y	'	□	□	□	(	ا	ا	ا	ا	ا	
1 0 1 0	10	end box <sup>(2)</sup>	separated graphics	*	□	:	□	J	Z	ا	□	□	□	ا	ا	ا	ا	ا	ا	
1 0 1 1	11	start box	TWIST	+	□	:	□	K	←	□	□	□	□	ا	ا	ا	ا	ا	ا	
1 1 0 0	12	normal height <sup>(2)</sup>	black back - ground <sup>(2)</sup>	,	□	<	□	L	½	ا	□	□	□	>	ا	ا	ا	ا	ا	
1 1 0 1	13	double height	new back - ground	-	□	=	□	M	→	□	□	□	□	ا	ا	ا	ا	ا	ا	
1 1 1 0	14	SO <sup>(1)</sup>	hold graphics	.	□	>	□	N	↑	ا	□	□	□	<	ا	ا	ا	ا	ا	
1 1 1 1	15	SI <sup>(1)</sup>	release graphics <sup>(2)</sup>	/	□	?	□	O	#	ا	□	□	□	?	ا	ا	ا	ا	ا	

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**Note for character version number (00100) see Register 11B.**

1. These control characters are reserved for compatibility with other data codes.
2. These control characters are presumed before each row begins.



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Table 13 SAA5246AP/S character data input decoding, English and Thai languages.

BITS	b <sub>8</sub> →				b <sub>7</sub> →				b <sub>6</sub> →				b <sub>5</sub> →				b <sub>4</sub> b <sub>3</sub> b <sub>2</sub> b <sub>1</sub>			
	0	0	0 or 1	0	0 or 1	0	0	0	0	0	1	1	0	0	1	1	0	0	1	1
row	column	0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15	
0 0 0 0	0	alpha - numerics black	graphics black	□	□	0	□	@	P	๑	□	p	□	๒	□	๒	๒	๒	๒	
0 0 0 1	1	alpha - numerics red	graphics red	!	□	1	□	A	Q	a	□	q	□	๓	□	๓	๓	๓	๓	
0 0 1 0	2	alpha - numerics green	graphics green	"	□	2	□	B	R	b	□	r	□	๔	□	๔	๔	๔	๔	
0 0 1 1	3	alpha - numerics yellow	graphics yellow	#	□	3	□	C	S	c	□	s	□	๕	□	๕	๕	๕	๕	
0 1 0 0	4	alpha - numerics blue	graphics blue	\$	□	4	□	D	T	d	□	t	□	๖	□	๖	๖	๖	๖	
0 1 0 1	5	alpha - numerics magenta	graphics magenta	%	□	5	□	E	U	e	□	u	□	๗	□	๗	๗	๗	๗	
0 1 1 0	6	alpha - numerics cyan	graphics cyan	&	□	6	□	F	V	f	□	v	□	๘	□	๘	๘	๘	๘	
0 1 1 1	7	alpha - numerics white	graphics white	'	□	7	□	G	W	g	□	w	□	๙	□	๙	๙	๙	๙	
1 0 0 0	8	flash	conceal display	(	□	8	□	H	X	h	□	x	□	๐	□	๐	๐	๐	๐	
1 0 0 1	9	steady**	contiguous graphics	)	□	9	□	I	Y	i	□	y	□	๑	□	๑	๑	๑	๑	
1 0 1 0	10	end box	separated graphics	*	□	:	□	J	Z	j	□	z	□	๒	□	๒	๒	๒	๒	
1 0 1 1	11	start box	TWIST	+	□	;	□	K	(	k	□	←	□	๓	□	๓	๓	๓	๓	
1 1 0 0	12	normal height	black back-ground	,	□	<	□	L	≡	l	□	↓	□	๔	□	๔	๔	๔	๔	
1 1 0 1	13	double height	new back-ground	-	□	=	□	M	๑	m	□	→	□	๕	□	๕	๕	๕	๕	
1 1 1 0	14	SO*	hold graphics	.	□	>	□	N	๑	n	□	↑	□	๖	□	๖	๖	๖	๖	
1 1 1 1	15	SI*	release graphics	/	□	?	□	O	๑	o	□	□	□	๗	□	๗	๗	๗	๗	

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Note For character version number (00111) see Register 11B.

- \* These control characters are reserved for compatibility with other data codes.
- \*\* These control characters are presumed before each row begins.

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**Notes to Table 6 - 13**

1. Control characters shown in Columns 0 and 1 are normally displayed as spaces.
2. Characters may be referred to by column and row, For example 2/5 refers to %.
3. Black represents displayed colour. White represents background.
4. The SAA5246A national option characters are illustrated in Table
5. Characters 8/6, 8/7, 9/5, 9/6 and 9/7 are special characters for combining with character 8/5 (E, H and T codes only. Characters 5/12, 5/13, 5/14 and 5/15 are combined with 5/11 (S code only).
6. National option characters will be displayed according to the setting of control bits C12 to C14. These will be mapped into the basic code table into positions shown in Table 8.
7. Columns 2a, 3a, 6a and 7a are displayed in graphics mode.

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Table 14 SAA5146A basic character matrix.

7/8				NC	NC	NC	NC	
7/0								
6/8								
6/0	NC							
5/8				NC	NC	NC	NC	NC
5/0								
4/8								
4/0	NC							
3/8								
3/0								
2/8								
2/0				NC	NC			
2/1								
2/2								
2/3	NC							
2/4	NC							
2/5								
2/6								
2/7								

Where: NC = national option character position.

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Table 15 SAA5246AP/E national option character set.

LANGUAGE	PHCB <sup>(1)</sup>			CHARACTER POSITION (COLUMN / ROW)												
	C12	C13	C14	2/3	2/4	4/0	5/11	5/12	5/13	5/14	5/15	6/0	7/11	7/12	7/13	7/14
ENGLISH	0	0	0	£	\$	@	←	½	→	↑	#	—	¼		¾	÷
GERMAN	0	0	1	#	\$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
SWEDISH	0	1	0	#	×	é	Ä	Ö	Å	Ü	_	é	ä	ö	å	ü
ITALIAN <sup>(2)</sup>	0	1	1	£	\$	é	°	ç	→	↑	#	ù	à	ò	è	ì
FRENCH	1	0	0	é	ï	à	ë	è	ù	î	#	è	ä	ö	ù	ç
SPANISH	1	0	1	ç	\$	í	á	é	í	ó	ú	¿	ü	ñ	è	à

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(1) PHCB are the Page Header Control Bits. Other combinations default to English.

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Table 16 SAA5246AP/H national option character set.

LANGUAGE	PHCB <sup>(1)</sup>			CHARACTER POSITION (COLUMN / ROW)												
	C12	C13	C14	2 / 3	2 / 4	4 / 0	5 / 11	5 / 12	5 / 13	5 / 14	5 / 15	6 / 0	7 / 11	7 / 12	7 / 13	7 / 14
POLISH	0	0	0	#	ń	ą	ź	ś	ł	ć	ó	ę	ż	ś	Ź	ź
GERMAN	0	0	1	#	ß	š	ä	ö	ü	^	□	°	ä	ö	ü	ß
SWEDISH	0	1	0	#	Å	É	Ä	Ö	Å	Ü	□	é	ä	ö	å	ü
SERBO-CROAT	1	0	1	#	љ	č	ć	ž	đ	š	ë	č	ć	ž	đ	š
CZECHOSLOVAKIA	1	1	0	#	ů	č	ť	ž	ý	í	ř	é	á	ě	ú	š
RUMANIAN	1	1	1	#	Å	Ț	Ă	Ș	Ă	Ț	Ț	ă	ș	ă	ț	î

MLA966

(1) PHCB are the Page Header Control Bits. Other combinations default to German. Only the above characters change with the PHCB. All other characters in the basic set are shown in Table 14.

Integrated VIP and Teletext (IVT1.0)

SAA5246A

Table 17 SAA5246AP/T national option character set.

LANGUAGE	PHCB <sup>(1)</sup>			CHARACTER POSITION (COLUMN / ROW)												
	C12	C13	C14	2 / 3	2 / 4	4 / 0	5 / 11	5 / 12	5 / 13	5 / 14	5 / 15	6 / 0	7 / 11	7 / 12	7 / 13	7 / 14
ENGLISH	0	0	0	€	\$	@	←	↳	→	↑	#	—	¼		¾	÷
GERMAN	0	0	1	#	\$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
TURKISH	1	1	0	ı	ç	ş	ö	ç	ü	ğ	ı	ş	ö	ç	ü	
ITALIAN	0	1	1	€	\$	é	°	ç	→	↑	#	ù	à	ò	è	ì
FRENCH	1	0	0	é	ï	à	ë	è	ù	î	#	é	à	ò	ù	ç
SPANISH	1	0	1	ç	\$	ı	á	é	í	ó	ú	ó	ü	ñ	è	à

MBA430

(1) PHCB are the Page Header Control Bits. Other combinations default to English. Only the above characters change with the PHCB. All other characters in the basic set are shown in Table 14.



Integrated VIP and Teletext (IVT1.0)

SAA5246A

Table 18 SAA5246AP/J national option character set.

LANGUAGE	PHCB <sup>(1)</sup>			CHARACTER POSITION (COLUMN / ROW)													
	C12	C13	C14	2/3	2/4	4/0	5/11	5/12	5/13	5/14	5/15	6/0	7/11	7/12	7/13	7/14	
SERBO-CROAT LATIN	0	1	0	#	Ě	Č	Ć	Ž	Đ	Š	ě	č	ć	ž	đ	š	
SERBO-CROAT LATIN	0	1	1	#	Ě	Č	Ć	Ž	Đ	Š	ě	č	ć	ž	đ	š	
HUNGARIAN SWEDISH	0	1	1	#	\$	É	Ä	Ö	Å	Ü	—	é	ä	ö	å	ü	
SERBO-CROAT LATIN	0	1	1	#	Ě	Č	Ć	Ž	Đ	Š	ě	č	ć	ž	đ	š	
SERBO-CROAT	0	1	1	#	Ě	Č	Ć	Ž	Đ	Š	ě	č	ć	ž	đ	š	
(RUMANIAN)	0	1	1	#	\$	Ț	Ă	Ș	Ă	Ț	ı	ț	ă	ș	ă	ț	
RUMANIAN	0	1	1	#	\$	Ț	Ă	Ș	Ă	Ț	ı	ț	ă	ș	ă	ț	
SERBO-CROATIC CYRILLIC	1	0	0		2	3	4	5	6	7							
			0	□	О	Ч	П	Ч	п								
		1	!	І	А	Ќ	а	ќ									
		2	”	2	Б	Р	б	р									
		3	#	3	Ц	С	ц	с									
		4	Ě	4	Д	Т	д	т									
		5	%	5	Е	У	е	у									
		6	&	6	Ф	В	ф	в									
		7	'	7	Г	Ѓ	г	ѓ									
		8	(	8	Х	Љ	х	љ									
		9	)	9	И	Њ	и	њ									
		10	*	:	Ј	З	ј	з									
		11	+	;	К	Ћ	к	ћ									
		12	,	<	Л	Ж	л	ж									
		13	-	=	М	Њ	м	њ									
		14	.	>	Н	Ш	н	ш									
		15	/	?	О	У	о	у	■								

MLA970

(1) PHCB are the Page Header Control Bits. Other combinations default to Serbo-Croat Latin.

Integrated VIP and Teletext (IVT1.0)

SAA5246A

Table 19 SAA5246AP/K national option character set.

	2	3	4	5	6	7		2	3	4	5	6	7
0	□	0	à	P	è	p	0	□	0	أ	ب	ج	د
1	!	1	A	Q	a	q	1	!	1	هـ	و	ز	ح
2	”	2	B	R	b	r	2	”	2	ط	ق	ك	غ
3	é	3	C	S	c	s	3	£	3	ب	س	ك	غ
4	ï	4	D	T	d	t	4	\$	4	ذ	ش	ل	ف
5	%	5	E	U	e	u	5	%	5	ت	م	م	ق
6	&	6	F	V	f	v	6	ل	6	ل	ن	ن	ق
7	'	7	G	W	g	w	7	ي	7	ا	ط	هـ	ك
8	(	8	H	X	h	x	8	)	8	ب	ظ	و	ا
9	)	9	I	Y	i	y	9	(	9	ة	ط	س	ل
10	*	:	J	Z	j	z	10	*	:	ن	ذ	ي	م
11	+	;	K	ë	k	â	11	+	;	ن	ذ	ث	م
12	,	<	L	è	l	ö	12	,	>	ج	ج	ج	ز
13	-	=	M	ù	m	û	13	-	=	ذ	ذ	ج	ن
14	.	>	N	î	n	ç	14	.	<	ا	ح	خ	لا
15	/	?	O	#	o	■	15	/	?	ا	#	ا	■
LANGUAGE	FRENCH						ARABIC						
PHCB <sup>(1)</sup> (C12, C13, C14)	1 0 0						1 1 1						

MLA968 - 1

(1) PHCB are the Page Header Control Bits. Other combinations default to French.

Integrated VIP and Teletext (IVT1.0)

SAA5246A

Table 20 SAA5246AP/L national option character set.

	2	3	4	5	6	7		2	3	4	5	6	7
0	□	0	@	P	N	J	0	□	0	ة	ا	ا	ا
1	!	1	A	Q	1	0	1	!	1	ء	و	ف	م
2	"	2	B	R	ا	U	2	"	2	ح	و	ق	ف
3	£	3	C	S	T	7	3	£	3	ب	س	ك	ف
4	\$	4	D	T	ا	9	4	\$	4	ذ	ش	ل	ف
5	%	5	E	U	1	Y	5	%	5	ت	م	م	ف
6	&	6	F	V	I	Y	6	ل	6	ا	ظ	ا	ف
7	'	7	G	W	ا	Q	7	ي	7	ا	ط	ه	ك
8	(	8	H	X	U	7	8	)	8	ح	ظ	و	ا
9	)	9	I	Y	'	W	9	(	9	ة	م	س	ل
10	*	:	J	Z	ا	ا	10	*	:	ا	ف	ب	م
11	+	;	K	←	□	□	11	+	:	ا	ف	ا	م
12	,	<	L	½	7		12	,	>	ح	ح	ح	ن
13	-	=	M	→	□	¼	13	-	=	ا	ا	ح	ن
14	.	>	N	↑	□	÷	14	.	<	ا	ا	ح	ا
15	/	?	O	#		■	15	/	?	ا	#	ا	■
LANGUAGE	HEBREW/ENGLISH						ARABIC						
PHCB <sup>(1)</sup> (C12, C13, C14)	1 0 1						1 1 1						

MLA967

(1) PHCB are the Page Header Control Bits. Other combinations default to Hebrew English.

Integrated VIP and Teletext (IVT1.0)

SAA5246A

Table 21 SAA5246AP/I national option character set.

	2	3	4	5	6	7		2	3	4	5	6	7
0	□	0	İ	P	ı	İ	0	□	0	İ	Π	Ü	π
1	!	1	A	Q	a	q	1	!	1	A	P	α	ρ
2	”	2	B	R	b	r	2	”	2	B	’	β	ς
3	İ	3	C	S	c	s	3	#	3	Γ	Σ	γ	σ
4	ğ	4	D	T	d	t	4	\$	4	Δ	T	δ	τ
5	%	5	E	U	e	u	5	%	5	E	Υ	ε	υ
6	&	6	F	V	f	v	6	&	6	Z	Φ	ζ	φ
7	’	7	G	W	g	w	7	’	7	H	Χ	η	χ
8	(	8	H	X	h	x	8	(	8	Θ	Ψ	θ	ψ
9	)	9	I	Y	i	y	9	)	9	I	Ω	ι	ω
10	*	:	J	Z	j	z	10	*	:	K	Ι	κ	ϊ
11	+	;	K	Ş	k	ş	11	+	;	Λ	Υ	λ	υ
12	,	<	L	Ö	l	ö	12	,	<	Μ	ά	μ	ό
13	-	=	M	Ç	m	ç	13	-	=	N	É	ν	ύ
14	.	>	N	Ü	n	ü	14	.	>	Ξ	ή	ξ	ώ
15	/	?	O	Ğ	o	■	15	/	?	Ο	ι	ο	■
LANGUAGE	TURKISH						GREEK						
PHCB <sup>(1)</sup> (C12, C13, C14)	1 1 0						1 1 1						

MLA969 - 1

(1) PHCB are the Page Header Control Bits. Other combinations default to Turkish.

Integrated VIP and Teletext (IVT1.0)

SAA5246A

Table 22 SAA5246AP/S national option character set (part A).

0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	10	11	12	13	14	14a	15	15a	
□	□	□	□	0	.	@	P	๑	.	p	□	๙	๘	□	0	l	๗	๘	.	๘	□	0
□	□	!	□	1	□	A	Q	a	□	q	□	+	๙	!	1	๗	๗	5	□	๘	□	1
□	□	"	□	2	□	B	R	b	□	r	□	/	๙	"	2	๗	๑	๗	□	๘	□	2
□	□	#	□	3	□	C	S	c	□	s	□	๘	๘	#	3	๗	๑	๗	□	๘	□	3
□	□	\$	□	4	□	D	T	d	□	t	□	๙	๘	\$	4	๗	๑	๗	□	'	□	4
□	□	%	□	5	□	E	U	e	□	u	□	๙	๘	%	5	๗	๑	๗	□	๘	□	5
□	□	&	□	6	□	F	V	f	□	v	□	๙	๘	&	6	๗	๑	๗	□	๘	□	6
□	□	'	□	7	□	G	W	g	□	w	□	๘	๘	'	7	๗	๑	๗	□	๘	□	7
□	□	(	□	8	□	H	X	h	□	x	□	๙	๘	(	8	๗	๑	๗	□	๘	□	8
□	□	)	□	9	□	I	Y	i	□	y	□	๙	๘	)	9	๗	๑	๗	□	๘	□	9
□	□	*	□	:	□	J	Z	j	□	z	□	๘	๘	*	:	๗	๑	๗	□	๘	□	10
□	□	+	□	;	□	K	€	k	□	+	□	๘	๘	+	;	๗	๑	๗	□	๘	□	11
□	□	,	□	<	□	L	๓	l	□	↓	□	๘	๘	,	<	๗	๑	๗	□	๘	□	12
□	□	-	□	=	□	M	๑	m	□	→	□	๙	๘	-	=	๗	๑	๗	□	.	□	13
□	□	.	□	>	□	N	๑	n	□	↑	□	๙	๘	.	>	๗	๑	๗	□	๘	□	14
□	□	/	□	?	□	O	๑	o	□	□	□	๘	๘	/	?	๗	๑	๗	□	๘	□	15

English ( 0 0 0 ) TWIST not invoked	PHCB <sup>(1)</sup> (C <sub>12</sub> , C <sub>13</sub> , C <sub>14</sub> )
OR	
Thai ( 0 1 0 ) and TWIST invoked	PHCB <sup>(1)</sup> (C <sub>12</sub> , C <sub>13</sub> , C <sub>14</sub> )

MLA971a

(1) PHCB are the Page Header Control Bits. Other combinations default to English.

Integrated VIP and Teletext (IVT1.0)

SAA5246A

Table 23 SAA5246AP/S national option character set (part B).

	0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	10	11	12	13	14	14a	15	15a	
0	□	□	□	□	0	□	๐	๑	๒	๓	๔	๕	๖	๗	๘	๙	๐	@	P	๑	□	p	□
1	□	□	!	□	1	□	๑	๒	๓	๔	๕	๖	๗	๘	๙	!	1	A	Q	a	□	q	□
2	□	□	"	□	2	□	๒	๓	๔	๕	๖	๗	๘	๙	"	2	B	R	b	□	r	□	□
3	□	□	#	□	3	□	๓	๔	๕	๖	๗	๘	๙	#	3	C	S	c	□	s	□	□	□
4	□	□	\$	□	4	□	๔	๕	๖	๗	๘	๙	\$	4	D	T	d	□	t	□	□	□	□
5	□	□	%	□	5	□	๕	๖	๗	๘	๙	%	5	E	U	e	□	u	□	□	□	□	□
6	□	□	&	□	6	□	๖	๗	๘	๙	&	6	F	V	f	□	v	□	□	□	□	□	□
7	□	□	'	□	7	□	๗	๘	๙	'	7	G	W	g	□	w	□	□	□	□	□	□	□
8	□	□	(	□	8	□	๘	๙	(	8	H	X	h	□	x	□	□	□	□	□	□	□	□
9	□	□	)	□	9	□	๙	)	9	I	Y	i	□	y	□	□	□	□	□	□	□	□	□
10	□	□	*	□	:	□	๑	๒	๓	๔	๕	๖	๗	๘	๙	*	:	J	Z	j	□	z	□
11	□	□	+	□	;	□	๑	๒	๓	๔	๕	๖	๗	๘	๙	+	;	K	€	k	□	←	□
12	□	□	,	□	<	□	๑	๒	๓	๔	๕	๖	๗	๘	๙	,	<	L	☰	l	□	↓	□
13	□	□	-	□	=	□	๑	๒	๓	๔	๕	๖	๗	๘	๙	-	=	M	๑	m	□	→	□
14	□	□	.	□	>	□	๑	๒	๓	๔	๕	๖	๗	๘	๙	.	>	N	๑	n	□	↑	□
15	□	□	/	□	?	□	๑	๒	๓	๔	๕	๖	๗	๘	๙	/	?	๐	๑	๒	๓	๔	๕

	Thai ( 0 1 0 ) TWIST not invoked
	OR
	English ( 0 0 0 ) and TWIST invoked

MLA971b

(1) PHCB are the Page Header Control Bits. Other combinations default to English.

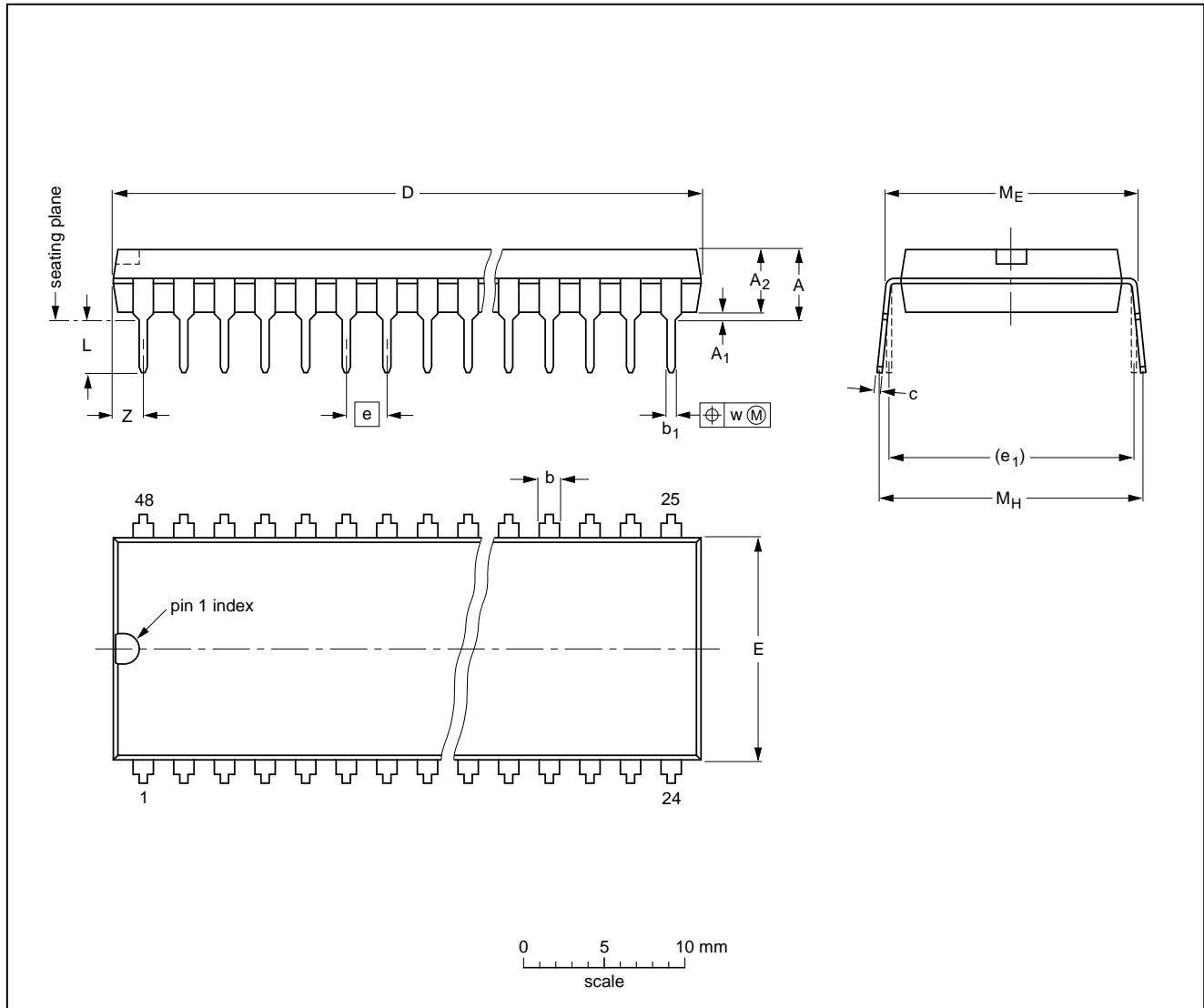
Integrated VIP and Teletext (IVT1.0)

SAA5246A

PACKAGE OUTLINES

DIP48: plastic dual in-line package; 48 leads (600 mil)

SOT240-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.9	0.36	4.06	1.4 1.14	0.53 0.38	0.36 0.23	62.60 61.60	14.22 13.56	2.54	15.24	3.90 3.05	15.88 15.24	18.46 15.24	0.254	2.1
inches	0.19	0.014	0.16	0.055 0.045	0.021 0.015	0.014 0.009	2.46 2.42	0.56 0.53	0.10	0.60	0.15 0.12	0.63 0.60	0.73 0.60	0.01	0.083

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

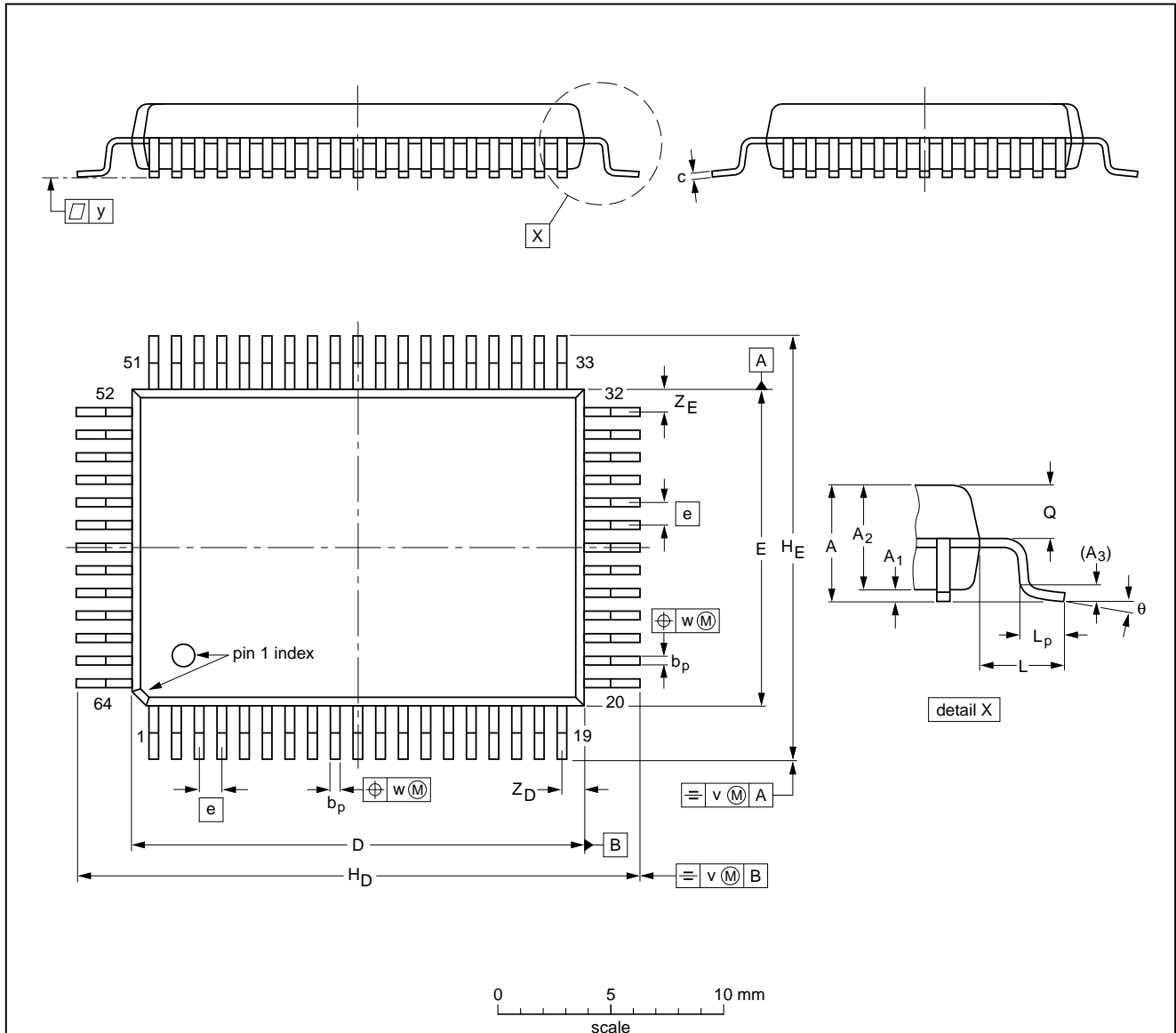
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT240-1						92-11-17 95-01-25

Integrated VIP and Teletext (IVT1.0)

SAA5246A

QFP64: plastic quad flat package; 64 leads (lead length 2.35 mm); body 14 x 20 x 2.8 mm

SOT319-3



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>D</sub>	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sub>D</sub> <sup>(1)</sup>	Z <sub>E</sub> <sup>(1)</sup>	θ
mm	3.25	0.30 0.10	2.90 2.65	0.25	0.50 0.35	0.25 0.14	20.1 19.9	14.1 13.9	1	25.0 24.4	19.0 18.4	2.35	1.4 1.0	1.4 1.2	0.2	0.2	0.1	1.2 0.8	1.2 0.8	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT319-3						94-03-22 95-02-04



## Integrated VIP and Teletext (IVT1.0)

SAA5246A

### SOLDERING

#### Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

#### SDIP

##### SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ( $T_{stg\ max}$ ). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

##### REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

#### QFP

##### REFLOW SOLDERING

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary from 50 to 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheat for 45 minutes at 45 °C.

##### WAVE SOLDERING

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

**If wave soldering cannot be avoided, the following conditions must be observed:**

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

**Even with these conditions, do not consider wave soldering the following packages: QFP52 (SOT379-1), QFP100 (SOT317-1), QFP100 (SOT317-2), QFP100 (SOT382-1) or QFP160 (SOT322-1).**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured. Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

##### REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

## Integrated VIP and Teletext (IVT1.0)

SAA5246A

**DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

**LIFE SUPPORT APPLICATIONS**

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

**PURCHASE OF PHILIPS I<sup>2</sup>C COMPONENTS**

Purchase of Philips I<sup>2</sup>C components conveys a license under the Philips' I<sup>2</sup>C patent to use the components in the I<sup>2</sup>C system provided the system conforms to the I<sup>2</sup>C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.