TEXAS INSTRUMENTS

TVP5150A/TVP5150AM1

Ultralow Power NTSC/PAL/SECAM Video Decoder With Robust Sync Detector

Data Manual

May 2004

HPA Digital Audio Video

SLES098

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1 Introduction

The TVP5150A device is an ultralow power NTSC/PAL/SECAM video decoder. Available in a space saving 32-pin TQFP package, the TVP5150A decoder converts NTSC, PAL, and SECAM video signals to 8-bit ITU-R BT.656 format. Discrete syncs are also available. The optimized architecture of the TVP5150A decoder allows for ultralow-power consumption. The decoder consumes 115 mW of power in typical operation and consumes less than 1 mW in power-down mode, considerably increasing battery life in portable applications. The decoder uses just one crystal for all supported standards. The TVP5150A decoder can be programmed using an I^2C serial interface. The decoder uses a 1.8-V supply for its analog and digital supplies, and a 3.3-V supply for its I/O.

The TVP5150A decoder converts baseband analog video into digital YCbCr 4:2:2 component video. Composite and S-video inputs are supported. The TVP5150A decoder includes one 9-bit analog-to-digital converter (ADC) with 2x sampling. Sampling is ITU-R BT.601 (27.0 MHz, generated from the 14.31818-MHz crystal or oscillator input) and is line-locked. The output formats can be 8-bit 4:2:2 or 8-bit ITU-R BT.656 with embedded synchronization.

The TVP5150A decoder utilizes Texas Instruments patented technology for locking to weak, noisy, or unstable signals. A Genlock/real-time control (RTC) output is generated for synchronizing downstream video encoders.

Complementary 4-line adaptive comb filtering is available for both the luma and chroma data paths to reduce both cross-luma and cross-chroma artifacts; a chroma trap filter is also available.

Video characteristics including hue, contrast, brightness, saturation, and sharpness may be programmed using the industry standard I^2C serial interface. The TVP5150A decoder generates synchronization, blanking, lock, and clock signals in addition to digital video outputs. The TVP5150A decoder includes methods for advanced vertical blanking interval (VBI) data retrieval. The VBI data processor slices, parses, and performs error checking on teletext, closed caption, and other data in several formats.

The TVP5150A decoder detects copy-protected input signals according to the Macrovision™ standard and detects Type 1, 2, 3, and colorstripe pulses.

The main blocks of the TVP5150A decoder include:

- Robust sync detector
- ADC with analog processor
- Y/C separation using 4-line adaptive comb filter
- Chrominance processor
- Luminance processor
- Video clock/timing processor and power-down control
- Output formatter
- I^2C interface
- VBI data processor
- Macrovision™ detection for composite and S-video

1.1 Features

- Accepts NTSC (M, 4.43), PAL (B, D, G, H, I, M, N), and SECAM (B, D, G, K, K1, L) video data
- Supports ITU-R BT.601 standard sampling
- High-speed 9-bit ADC
- Two composite inputs or one S-video input

- Fully differential CMOS analog preprocessing channels with clamping and automatic gain control (AGC) for best signal-to-noise (S/N) performance
- Ultralow power consumption: 115 mW typical
- 32-pin TQFP package
- Power-down mode: <1 mW
- Brightness, contrast, saturation, hue, and sharpness control through I^2C
- Complementary 4-line (3-H delay) adaptive comb filters for both cross-luminance and cross-chrominance noise reduction
- Patented architecture for locking to weak, noisy, or unstable signals
- Single 14.31818-MHz crystal for all standards
- Internal phase-locked loop (PLL) for line-locked clock and sampling
- Subcarrier Genlock output for synchronizing color subcarrier of external encoder
- Standard programmable video output format:
  - ITU-R BT.656, 8-bit 4:2:2 with embedded syncs
  - 8-bit 4:2:2 with discrete syncs
- Macrovision™ copy protection detection
- Advanced programmable video output formats:
  - 2x oversampled raw VBI data during active video
  - Sliced VBI data during horizontal blanking or active video
- VBI modes supported
  - Teletext (NABTS, WST)
  - Closed-caption decode with FIFO, and extended data services (EDS)
  - Wide screen signaling, video program system, CGMS, vertical interval time code
  - Gemstar 1x/2x electronic program guide compatible mode
  - Custom configuration mode that allows the user to program the slice engine for unique VBI data signals
- Power-on reset

1.2 Product Family

This data manual covers three devices in the TVP5150A product family: the TVP5150APBS, the TVP5150AM1PBS, and the TVP5150AM1ZQC. The hardware for these three devices is identical. The following software changes are the differences between these two devices. For the remainder of this document, unless otherwise noted, TVP5150A refers to all three devices.

- TVP5150APBS
  - ROM version 3.21
  - SECAM is masked from the autoswitch process in the default mode of register 0x04
  - Only supports ITU-R BT656.4 timing
- TVP5150AM1PBS/TVP5150AM1ZQC
  - ROM version 4.00
  - SECAM is unmasked from the autoswitch process in the default mode of register 0x04
  - Addition of register 0x30 to select ITU-R BT656.3 or ITU-R BT656.4 timing

1.3 Applications

The following is a partial list of suggested applications:

- Digital television
- PDA
- Notebook PCs
- Cell phones
- Video recorder/players
- Internet appliances/web pads
- Handheld games

1.4 Related Products

- *TVP5146 NTSC/PAL/SECAM 4x10-Bit Digital Video Decoder With Macrovision™ Detection, YPbPr/RGB Inputs, 5-Line Comb Filter and SCART/Digital RGB Overlay SupportDecoder With Robust Sync Detector*, Literature Number SLES084

1.5 Ordering Information

T_A	PACKAGED DEVICES	PACKAGE OPTION
	32TQFP-PBS	
0°C to 70°C	TVP5150APBS	Tray
0°C to 70°C	TVP5150APBSR	Tape and reel
0°C to 70°C	TVP5150AM1PBS	Tray
0°C to 70°C	TVP5150AM1PBSR	Tape and reel
0°C to 70°C	TVP5150AM1ZQC	Tray
0°C to 70°C	TVP5150AM1ZQCR	Tape and reel

1.6 Functional Block Diagram

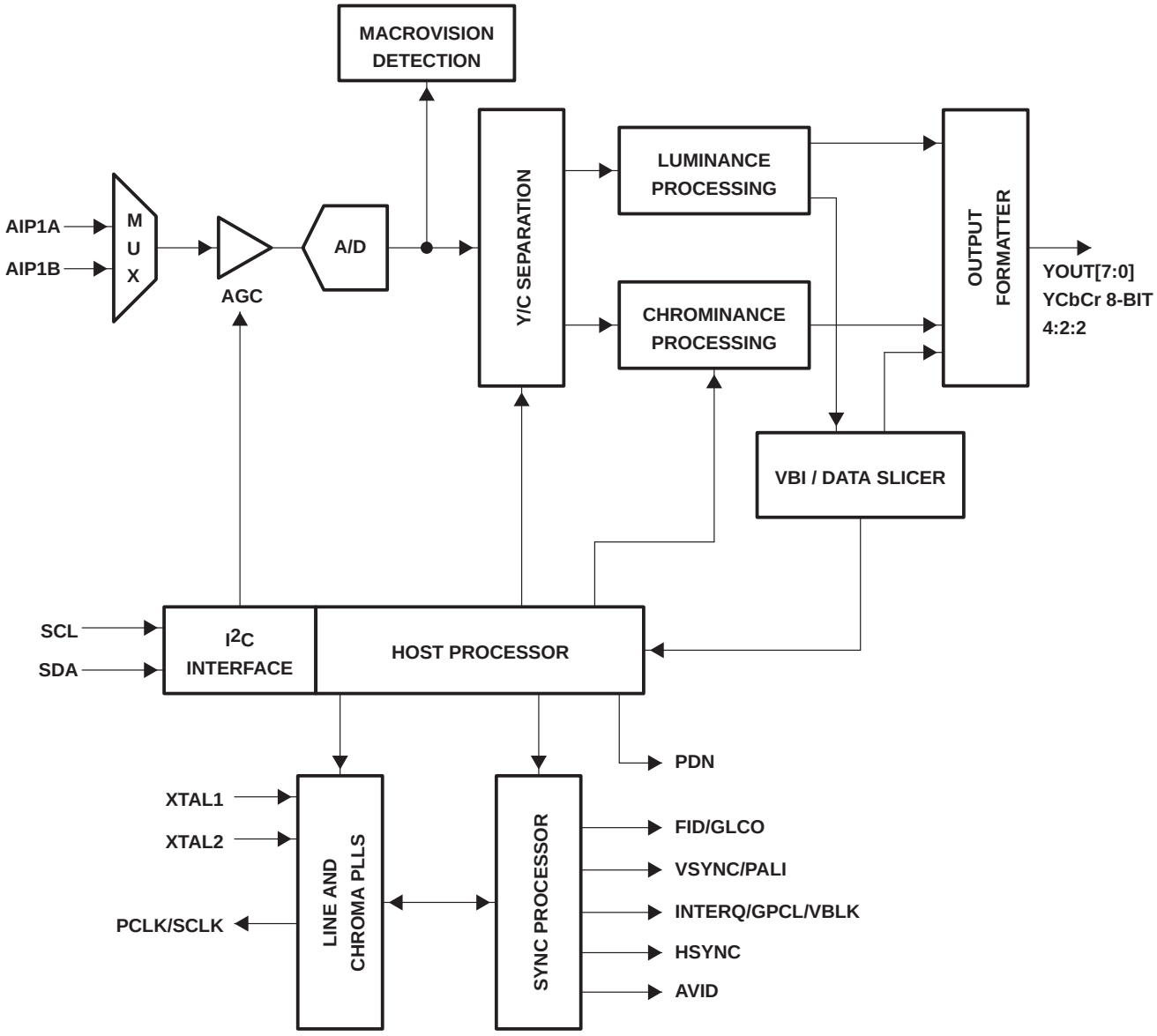
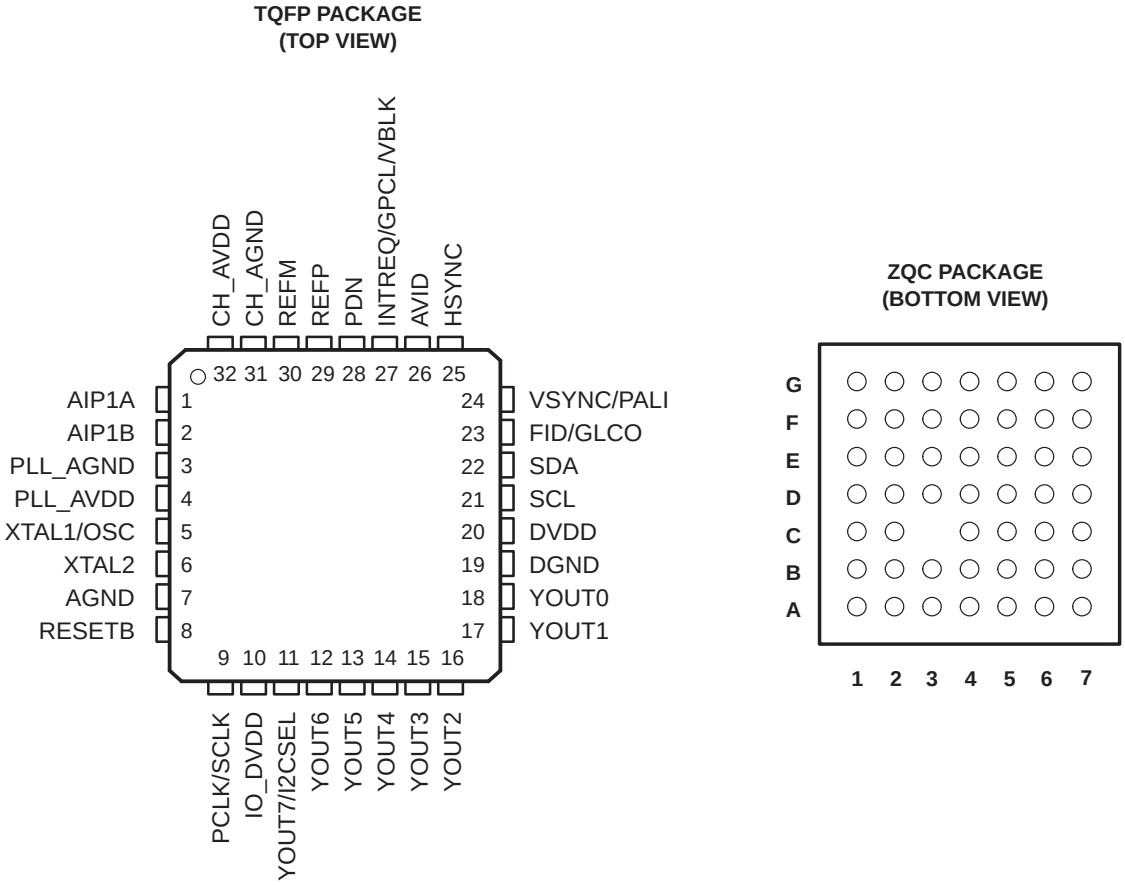


Figure 1−1. Functional Block Diagram

1.7 Terminal Assignments



1.8 Terminal Functions

Table 1−1. Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	NUMBER			
	PBS	ZQC		
Analog Section				
AGND	7	E1	I	Substrate. Connect to analog ground.
AIP1A	1	A1	I	Analog input. Connect to the video analog input via 0.1-µF capacitor. The maximum input range is 0−0.75 V_{PP}, and may require an attenuator to reduce the input amplitude to the desired level. If not used, connect to AGND via 0.1-µF capacitor. Refer to Figure 5−1.
AIP1B	2	B1	I	Analog input. Connect to the video analog input via 0.1-µF capacitor. The maximum input range is 0−0.75 V_{PP}, and may require an attenuator to reduce the input amplitude to the desired level. If not used, connect to AGND via 0.1-µF capacitor. Refer to Figure 5−1.
CH_AGND	31	A3	I	Analog ground
CH_AVDD	32	A2	I	Analog supply. Connect to 1.8-V analog supply.
NC	−	B2, B3, B6, C4, C5, D3−D6, E2−E5, F2, F5, F6	−	No connect
PLL_AGND	3	C2	I	PLL ground. Connect to analog ground.
PLL_AVDD	4	C1	I	PLL supply. Connect to 1.8-V analog supply.

Table 1−1. Terminal Functions (Continued)

TERMINAL			I/O	DESCRIPTION
NAME	NUMBER			
	PBS	ZQC		
Analog Section (continued)				
REFM	30	A4	I	A/D reference ground. Connect to analog ground through 1-µF capacitor. Also, it is recommended to connect directly to REFP through 1-µF capacitor. Refer to Figure 5−1.
REFP	29	B4	I	A/D reference supply. Connect to analog ground through 1-µF capacitor. Refer to Figure 5−1.
Digital Section				
AVID	26	A6	O	Active video indicator. This signal is high during the horizontal active time of the video output. AVID toggling during vertical blanking intervals is controlled by bit 2 of the active video cropping start pixel LSB register at address 12h (see Section 2.20.17).
DGND	19	E6	I	Digital ground
DVDD	20	E7	I	Digital supply. Connect to 1.8-V digital supply
FID/GLCO	23	C6	O	FID: Odd/even field indicator or vertical lock indicator. For the odd/even indicator, a 1 indicates the odd field. GLCO: This serial output carries color PLL information. A slave device can decode the information to allow chroma frequency control from the TVP5150A decoder. Data is transmitted at the SCLK rate in Genlock mode. In RTC mode, SCLK/4 is used.
HSYNC	25	A7	O	Horizontal synchronization signal
INTREQ/GPCL/ VBLK	27	B5	I/O	INTREQ: Interrupt request output. GPCL/VBLK: General-purpose control logic. This terminal has two functions: 1. GPCL: General-purpose output. In this mode the state of GPCL is directly programmed via I^2C. 2. VBLK: Vertical blank output. In this mode the GPCL terminal indicates the vertical blanking interval of the output video. The beginning and end times of this signal are programmable via I^2C.
IO_DVDD	10	G2	I	Digital supply. Connect to 3.3 V.
PCLK/SCLK	9	G1	O	System clock at either 1x or 2x the frequency of the pixel clock.
PDN	28	A5	I	Power-down terminal (active low). Puts the decoder in standby mode. Preserves the value of the registers.
RESETB	8	F1	I	Active-low reset. RESETB can be used only when PDN = 1. When RESETB is pulled low, it resets all the registers and restarts the internal microprocessor.
SCL	21	D7	I/O	I^2C serial clock (open drain)
SDA	22	C7	I/O	I^2C serial data (open drain)
VSYNC/PALI	24	B7	O	VSYNC: Vertical synchronization signal PALI: PAL line indicator or horizontal lock indicator For the PAL line indicator: 1 = Indicates a noninverted line 0 = Indicates an inverted line
XTAL1/OSC XTAL2	5 6	D2 D1	I O	External clock reference. The user may connect XTAL1 to an oscillator or to one terminal of a crystal oscillator. The user may connect XTAL2 to the other terminal of the crystal oscillator or not connect XTAL2 at all. One single 14.31818-MHz crystal or oscillator is needed for ITU-R BT.601 sampling, for all supported standards.
YOUT[6:0]	12 13 14 15 16 17 18	G3 F4 G4 G5 G6 G7 F7	I/O	Output decoded ITU-R BT.656 output/YCbCr 4:2:2 output with discrete sync.
YOUT7/I2CSEL	11	F3	I/O	I2CSEL: Determines address for I^2C (sampled during reset). A pullup or pulldown register is needed (>1 kΩ) to program the terminal to the desired address. 1 = Address is 0xBA 0 = Address is 0xB8 YOUT7: MSB of output decoded ITU-R BT.656 output/YCbCr 4:2:2 output.

2 Functional Description

2.1 Analog Front End

The TVP5150A decoder has an analog input channel that accepts two video inputs, which are ac-coupled. The decoder supports a maximum input voltage range of 0.75 V; therefore, an attenuation of one-half is needed for most input signals with a peak-to-peak variation of 1.5 V. The maximum parallel termination before the input to the device is 75 Ω. Please refer to the applications diagram in Figure 5−1 for the recommended configuration. The two analog input ports can be connected as follows:

- Two selectable composite video inputs or
- One S-video input

An internal clamping circuit restores the ac-coupled video signal to a fixed dc level.

The programmable gain amplifier (PGA) and the AGC circuit work together to make sure that the input signal is amplified sufficiently to ensure the proper input range for the ADC.

The ADC has 9 bits of resolution and runs at a maximum speed of 27 MHz. The clock input for the ADC comes from the PLL.

2.2 Composite Processing Block Diagram

The composite processing block processes NTSC/PAL/SECAM signals into the YCbCr color space. Figure 2−1 explains the basic architecture of this processing block.

Figure 2−1 illustrates the luminance/chrominance (Y/C) separation process in the TVP5150A decoder. The composite video is multiplied by subcarrier signals in the quadrature modulator to generate the color difference signals Cb and Cr. Cb and Cr are then low-pass (LP) filtered to achieve the desired bandwidth and to reduce crosstalk.

An adaptive 4-line comb filter separates CbCr from Y. Chroma is remodulated through another quadrature modulator and subtracted from the line-delayed composite video to generate luma. Contrast, brightness, hue, saturation, and sharpness (using the peaking filter) are programmable via I^2C.

The Y/C separation is bypassed for S-video input. For S-video, the remodulation path is disabled.

2.3 Adaptive Comb Filtering

The 4-line comb filter can be selectively bypassed in the luma or chroma path. If the comb filter is bypassed in the luma path, then chroma notch filters are used. TI's patented adaptive 4-line comb filter algorithm reduces artifacts such as hanging dots at color boundaries and detects and properly handles false colors in high frequency luminance images such as a multiburst pattern or circle pattern.

2.4 Color Low-Pass Filter

In some applications, it is desirable to limit the Cb/Cr bandwidth to avoid crosstalk. This is especially true in case of video signals that have asymmetrical Cb/Cr sidebands. The color LP filters provided limit the bandwidth of the Cb/Cr signals.

Color LP filters are needed when the comb filtering turns off, due to extreme color transitions in the input image. Please refer to Section 2.20.25, *Chrominance Control #2 Register*, for the response of these filters. The filters have three options that allow three different frequency responses based on the color frequency characteristics of the input video.

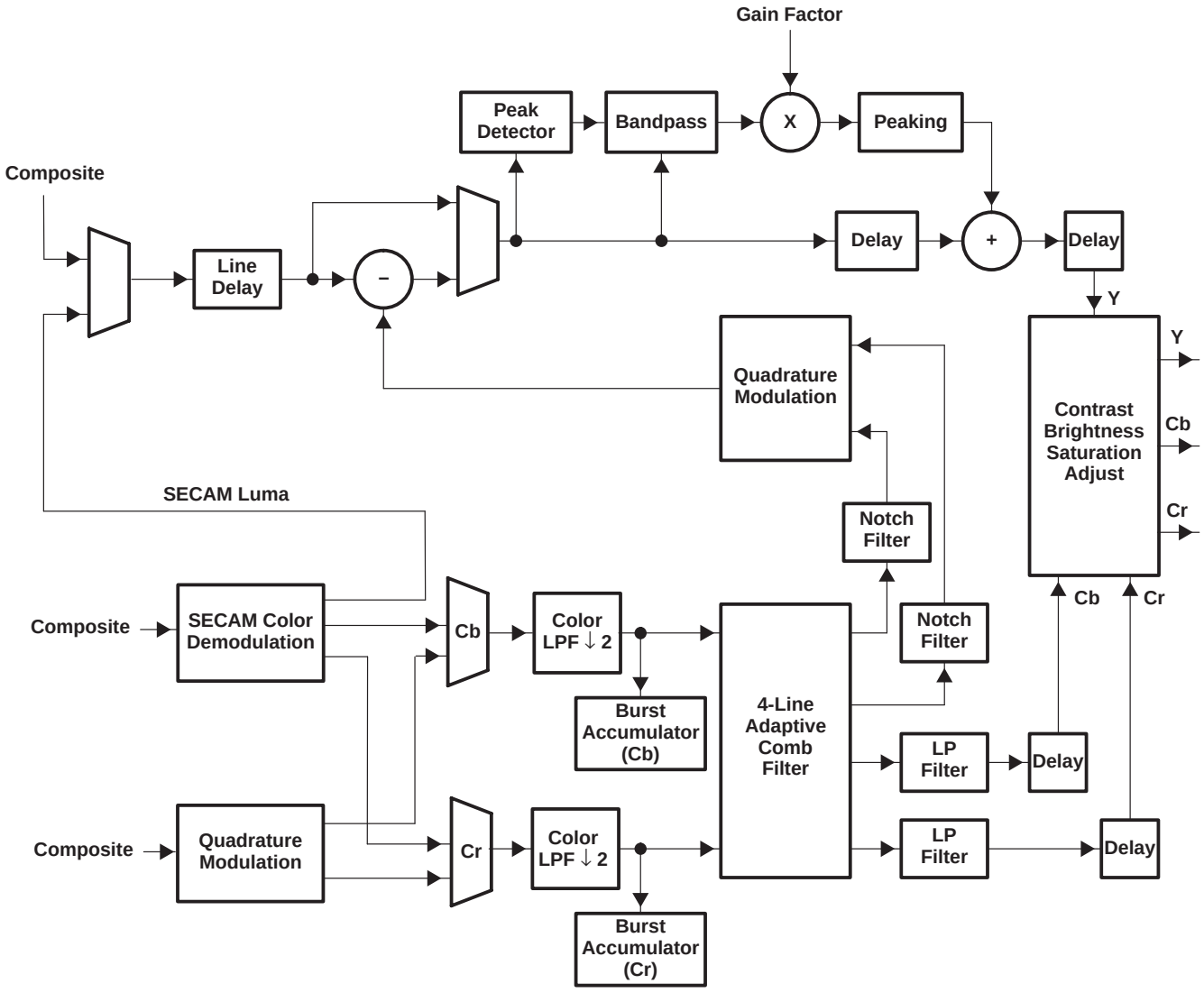


Figure 2−1. Composite Processing Block Diagram

2.5 Luminance Processing

The luma component is derived from the composite signal by subtracting the remodulated chroma information. A line delay exists in this path to compensate for the line delay in the adaptive comb filter in the color processing chain. The luma information is then fed into the peaking circuit, which enhances the high frequency components of the signal, thus improving sharpness.

2.6 Chrominance Processing

For NTSC/PAL formats, the color processing begins with a quadrature demodulator. The Cb/Cr signals then pass through the gain control stage for chroma saturation adjustment. An adaptive comb filter is applied to the demodulated signals to separate chrominance and eliminate cross-chrominance artifacts. An automatic color killer circuit is also included in this block. The color killer suppresses the chroma processing when the color burst of the video signal is weak or not present. The SECAM standard is similar to PAL except for the modulation of color which is FM instead of QAM.

2.7 Timing Processor

The timing processor is a combination of hardware and software running in the internal microprocessor that serves to control horizontal lock to the input sync pulse edge, AGC and offset adjustment in the analog front end, vertical sync detection, and Macrovision™ detection.

2.8 VBI Data Processor

The TVP5150A VBI data processor (VDP) slices various data services like teletext (WST, NABTS), closed caption (CC), wide screen signaling (WSS), etc. These services are acquired by programming the VDP to enable standards in the VBI. The results are stored in a FIFO and/or registers. The teletext results are stored in a FIFO only. Table 2−1 lists a summary of the types of VBI data supported according to the video standard. It supports ITU-R BT. 601 sampling for each.

Table 2−1. Data Types Supported by the VDP

LINE MODE REGISTER (D0h−FCh) BITS [3:0]	SAMPLING RATE (0Dh) BIT 7	NAME	DESCRIPTION
0000b	x	x	Reserved
0000b	1	WST SECAM 6	Teletext, SECAM
0001b	x	x	Reserved
0001b	1	WST PAL B 6	Teletext, PAL, System B
0010b	x	x	Reserved
0010b	1	WST PAL C 6	Teletext, PAL, System C
0011b	x	x	Reserved
0011b	1	WST, NTSC B 6	Teletext, NTSC, System B
0100b	x	x	Reserved
0100b	1	NABTS, NTSC C 6	Teletext, NTSC, System C
0101b	x	x	Reserved
0101b	1	NABTS, NTSC D 6	Teletext, NTSC, System D (Japan)
0110b	x	x	Reserved
0110b	1	CC, PAL 6	Closed caption PAL
0111b	x	x	Reserved
0111b	1	CC, NTSC 6	Closed caption NTSC
1000b	x	x	Reserved
1000b	1	WSS, PAL 6	Wide-screen signal, PAL
1001b	x	x	Reserved
1001b	1	WSS, NTSC 6	Wide-screen signal, NTSC
1010b	x	x	Reserved
1010b	1	VITC, PAL 6	Vertical interval timecode, PAL
1011b	x	x	Reserved
1011b	1	VITC, NTSC 6	Vertical interval timecode, NTSC
1100b	x	x	Reserved
1100b	1	VPS, PAL 6	Video program system, PAL
1101b	x	x	Reserved
1110b	x	x	Reserved
1111b	x	Active Video	Active video/full field

At powerup the host interface is required to program the VDP-configuration RAM (VDP-CRAM) contents with the lookup table (see Section 2.20.58). This is done through port address C3h. Each read from or write to this address will auto increment an internal counter to the next RAM location. To access the VDP-CRAM, the line mode registers (D0h−FCh) must be programmed with FFh to avoid a conflict with the internal microprocessor and the VDP in both writing and reading. Full field mode must also be disabled.

Available VBI lines are from line 6 to line 27 of both field 1 and field 2. Each line can be any VBI mode.

Output data is available either through the VBI-FIFO (B0h) or through dedicated registers at 90h−AFh, both of which are available through the I^2C port.

2.9 VBI FIFO and Ancillary Data in Video Stream

Sliced VBI data can be output as ancillary data in the video stream in the ITU-R BT.656 mode. VBI data is output during the horizontal blanking period following the line from which the data was retrieved. Table 2−2 shows the header format and sequence of the ancillary data inserted into the video stream. This format is also used to store any VBI data into the FIFO. The size of FIFO is 512 bytes. Therefore, the FIFO can store up to 11 lines of teletext data with the NTSC NABTS standard.

Table 2−2. Ancillary Data Format and Sequence

BYTE NO.	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)	DESCRIPTION	
0	0	0	0	0	0	0	0	0	Ancillary data preamble	
1	1	1	1	1	1	1	1	1		
2	1	1	1	1	1	1	1	1		
3	NEP	EP	0	1	0	DID2	DID1	DID0	Data ID (DID)	
4	NEP	EP	F5	F4	F3	F2	F1	F0	Secondary data ID (SDID)	
5	NEP	EP	N5	N4	N3	N2	N1	N0	Number of 32 bit data (NN)	
6	Video line # [7:0]								Internal data ID0 (IDID0)	
7	0	0	0	Data error	Match #1	Match #2	Video line # [9:8]		Internal data ID1 (IDID1)	
8	1. Data								Data byte	1st word
9	2. Data								Data byte	
10	3. Data								Data byte	
11	4. Data								Data byte	
:	:								:	
	m−1. Data								Data byte	Nth word
	m. Data								Data byte	
	NEP	EP	CS[5:0]						Check sum	
4(N+2)−1	1	0	0	0	0	0	0	0	Fill byte	

EP: Even parity for D0−D5 NEP: Negated even parity

DID: 91h: Sliced data of VBI lines of first field
53h: Sliced data of line 24 to end of first field
55h: Sliced data of VBI lines of second field
97h: Sliced data of line 24 to end of second field

SDID: This field holds the data format taken from the line mode register of the corresponding line.

NN: Number of Dwords beginning with byte 8 through 4(N+2). This value is the number of Dwords where each Dword is 4 bytes.

IDID0: Transaction video line number [7:0]

IDID1: Bit 0/1 = Transaction video line number [9:8]
Bit 2 = Match 2 flag
Bit 3 = Match 1 flag
Bit 4 = 1 if an error was detected in the EDC block. 0 if not.

CS: Sum of D0−D7 of DID through last data byte.

Fill byte: Fill bytes make a multiple of 4 bytes from byte 0 to last fill byte. For teletext modes, byte 8 is the sync pattern byte. Byte 9 is 1. Data (the first data byte).

2.10 Raw Video Data Output

The TVP5150A decoder can output raw A/D video data at 2x sampling rate for external VBI slicing. This is transmitted as an ancillary data block during the active horizontal portion of the line and during vertical blanking.

2.11 Output Formatter

The YCbCr digital output can be programmed as 8-bit 4:2:2 or 8-bit ITU-R BT.656 parallel interface standard.

Table 2−3. Summary of Line Frequencies, Data Rates, and Pixel Counts

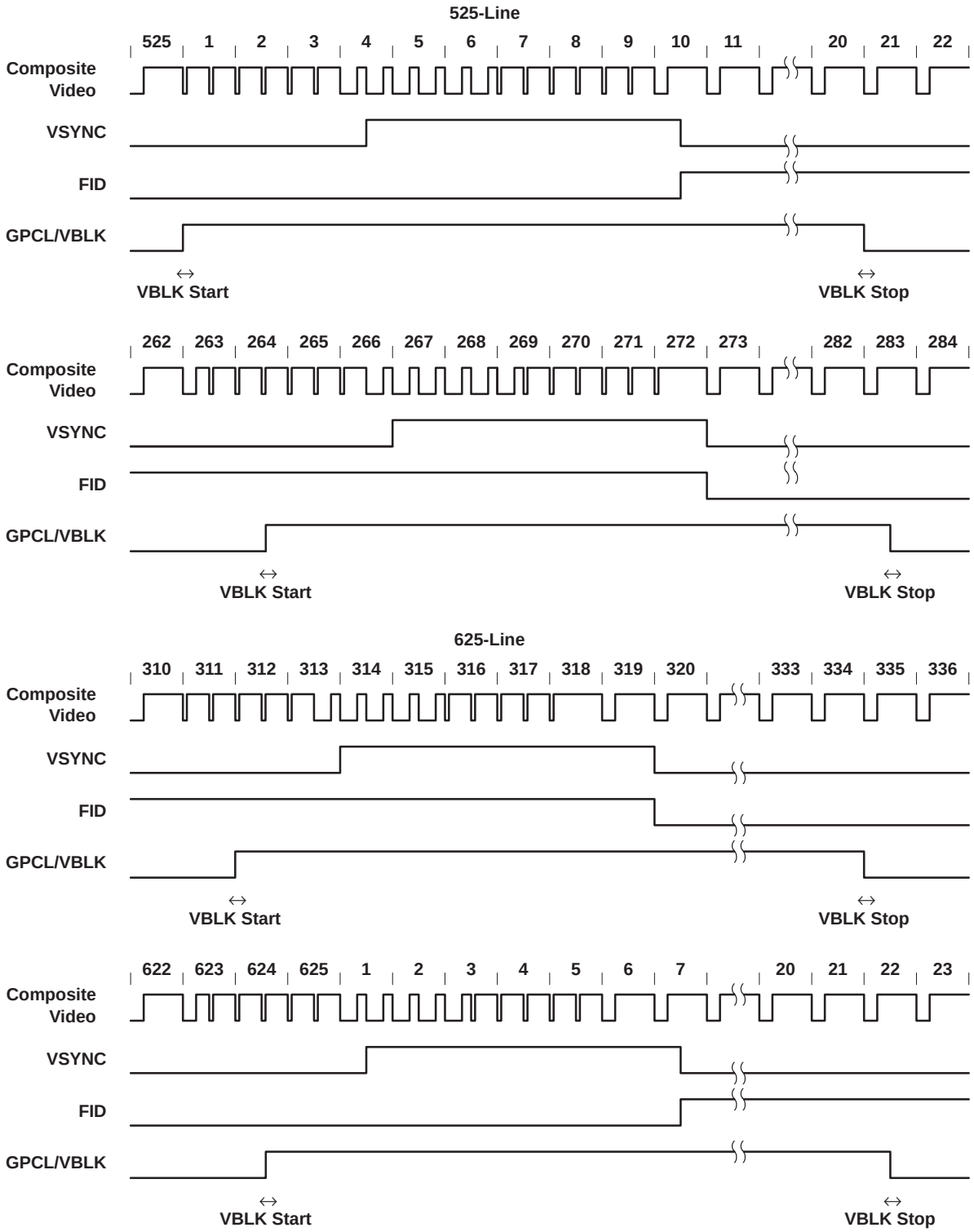
STANDARDS	HORIZONTAL LINE RATE (kHz)	PIXELS PER LINE	ACTIVE PIXELS PER LINE	SCLK FREQUENCY (MHz)
NTSC (M, 4.43), ITU-R BT.601	15.73426	858	720	27.00
PAL (B, D, G, H, I), ITU-R BT.601	15.625	864	720	27.00
PAL (M), ITU-R BT.601	15.73426	858	720	27.00
PAL (N), ITU-R BT.601	15.625	864	720	27.00
SECAM, ITU-R BT.601	15.625	864	720	27.00

2.12 Synchronization Signals

External (discrete) syncs are provided via the following signals:

- VSYNC (vertical sync)
- FID/VLK (field indicator or vertical lock indicator)
- GPCL/VBLK (general-purpose I/O or vertical blanking indicator)
- PALI/HLK (PAL switch indicator or horizontal lock indicator)
- HSYNC (horizontal sync)
- AVID (active video indicator)

VSYNC, FID, PALI, and VBLK are software-set and programmable to the SCLK pixel count. This allows any possible alignment to the internal pixel count and line count. The default settings for a 525-/625-line video output are given as an example below.

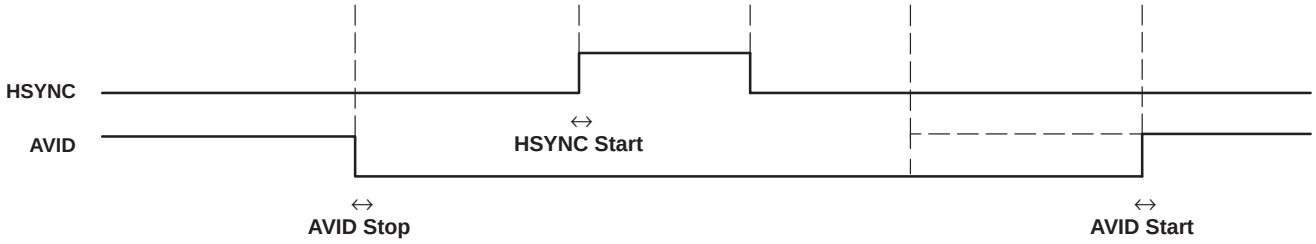


NOTE: Line numbering conforms to ITU-R BT.470.

Figure 2−2. 8-bit 4:2:2, Timing With 2x Pixel Clock (SCLK) Reference

ITU-R BT.656 timing.

NTSC 601	1436	1437	1438	1439	1440	1441	…	1455	1456	…	1583	1584	⋯	1711	1712	1713	1714	1715	0	1	2	3
PAL 601	1436	1437	1438	1439	1440	1441	…	1459	1460	…	1587	1588	⋯	1723	1724	1725	1726	1727	0	1	2	3
SECAM	1436	1437	1438	1439	1440	1441	…	1479	1480	…	1607	1608	⋯	1719	1720	1721	1722	1723	1724	1725	1726	1727
ITU 656 Datastream	Cb 359	Y 718	Cr 359	Y 719	FF	00	…	10	80	…	10	80	⋯	10	FF	00	00	XX	Cb 0	Y 0	Cr 0	Y 1



NOTE: AVID rising edge occurs 4 SCLK cycles early when in the ITU-R BT.656 output mode.

Figure 2−3. Horizontal Synchronization Signals

2.13 AVID Cropping

AVID or active video cropping provides a means to decrease bandwidth of the video output. This is accomplished by horizontally blanking a number of AVID pulses and by vertically blanking a number of lines per frame. The horizontal AVID cropping is controlled using registers 11h and 12h for start pixels MSB and LSB, respectively.

Registers 13h and 14h provide access to stop pixels MSB and LSB, respectively. The vertical AVID cropping is controlled using the vertical blanking (VBLK) start and stop registers at addresses 18h and 19h. Figure 2−4 shows an AVID application.

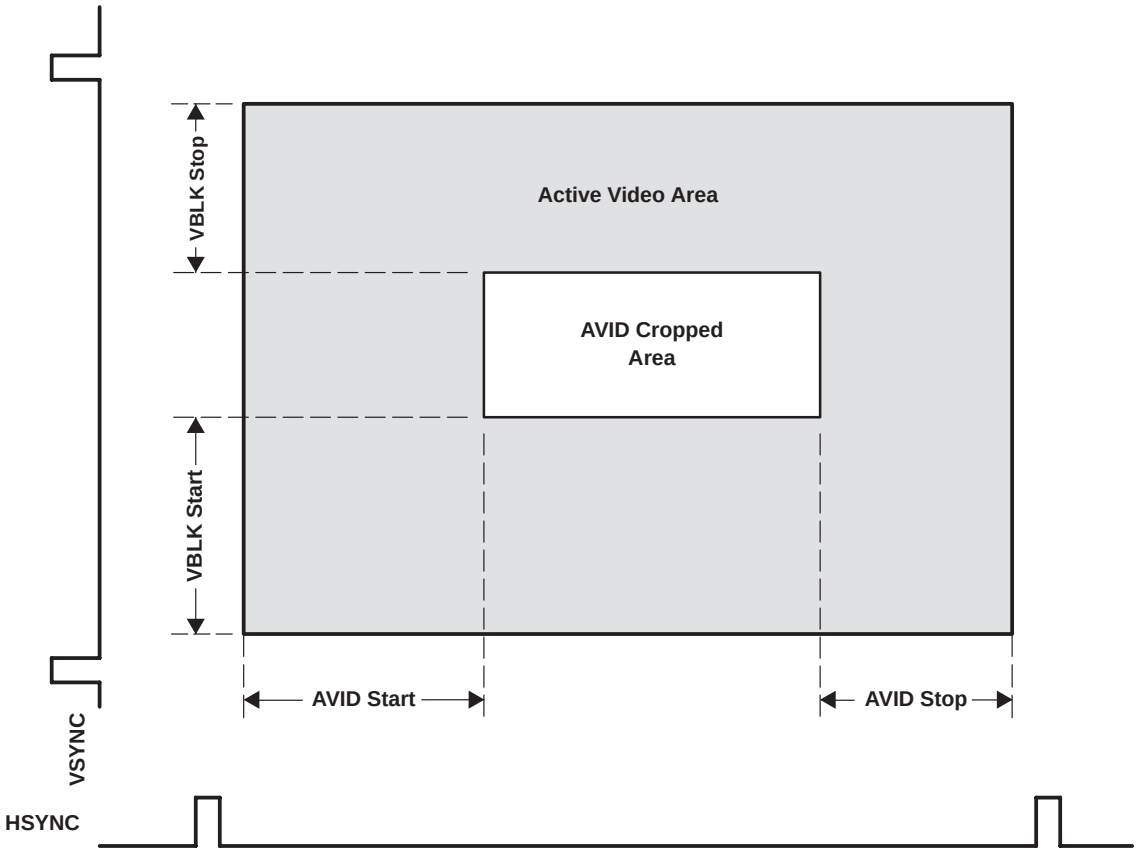


Figure 2−4. AVID Application

2.14 Embedded Syncs

Standards with embedded syncs insert SAV and EAV codes into the datastream at the beginning and end of horizontal blanking. These codes contain the V and F bits which also define vertical timing. F and V change on EAV. Table 2−4 gives the format of the SAV and EAV codes.

H equals 1 always indicates EAV. H equals 0 always indicates SAV. The alignment of V and F to the line and field counter varies depending on the standard. Please refer to ITU-R BT.656 for more information on embedded syncs.

The P bits are protection bits:

P3 = V xor H
P2 = F xor H
P1 = F xor V
P0 = F xor V xor H

Table 2−4. EAV and SAV Sequence

	8-BIT DATA							
	D7 (MSB)	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Preamble	1	1	1	1	1	1	1	1
Preamble	0	0	0	0	0	0	0	0
Preamble	0	0	0	0	0	0	0	0
Status word	1	F	V	H	P3	P2	P1	P0

2.15 I²C Host Interface

The I²C standard consists of two signals, serial input/output data line (SDA) and input/output clock line (SCL), which carry information between the devices connected to the bus. A third signal (I2CSEL) is used for slave address selection. Although the I²C system can be multimastered, the TVP5150A decoder functions as a slave device only.

Both SDA and SCL must be connected to a positive supply voltage via a pullup resistor. When the bus is free, both lines are high. The slave address select terminal (I2CSEL) enables the use of two TVP5150A decoders tied to the same I²C bus. At power up, the status of the I2CSEL is polled. Depending on the write and read addresses to be used for the TVP5150A decoder, it can either be pulled low or high through a resistor. This terminal is multiplexed with YOUT7 and hence must not be tied directly to ground or IO_DVDD. Table 2−6 summarizes the terminal functions of the I²C-mode host interface.

Table 2−5. Write Address Selection

I2CSEL	WRITE ADDRESS
0	B8h
1	BAh

Table 2−6. I²C Terminal Description

SIGNAL	TYPE	DESCRIPTION
I2CSEL (YOUT7)	I	Slave address selection
SCL	I/O (open drain)	Input/output clock line
SDA	I/O (open drain)	Input/output data line

Data transfer rate on the bus is up to 400 kbits/s. The number of interfaces connected to the bus is dependent on the bus capacitance limit of 400 pF. The data on the SDA line must be stable during the high period of the SCL except for start and stop conditions. The high or low state of the data line can only change with the clock signal on the SCL line being low. A high-to-low transition on the SDA line while the SCL is high indicates an I²C start condition. A low-to-high transition on the SDA line while the SCL is high indicates an I²C stop condition.

Every byte placed on the SDA must be 8 bits long. The number of bytes which can be transferred is unrestricted. Each byte must be followed by an acknowledge bit. The acknowledge-related clock pulse is generated by the I²C master.

2.15.1 I²C Write Operation

Data transfers occur utilizing the following illustrated formats.

An I²C master initiates a write operation to the TVP5150A decoder by generating a start condition (S) followed by the TVP5150A I²C address (as shown below), in MSB first bit order, followed by a 0 to indicate a write cycle. After receiving an acknowledge from the TVP5150A decoder, the master presents the subaddress of the register, or the first of a block of registers it wants to write, followed by one or more bytes of data, MSB first. The TVP5150A decoder acknowledges each byte after completion of each transfer. The I²C master terminates the write operation by generating a stop condition (P).

Step 1	**0**
I²C Start (master)	S

Step 2	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I²C General address (master)	1	0	1	1	1	0	X	0

Step 3	**9**
I²C Acknowledge (slave)	A

Step 4	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I²C Write register address (master)	addr	addr	addr	addr	addr	addr	addr	addr

Step 5	9
I2C Acknowledge (slave)	A

Step 6	7	6	5	4	3	2	1	0
I2C Write data (master)	Data	Data	Data	Data	Data	Data	Data	Data

Step 7†	9
I2C Acknowledge (slave)	A

Step 8	0
I2C Stop (master)	P

† Repeat steps 6 and 7 until all data have been written.

2.15.2 I2C Read Operation

The read operation consists of two phases. The first phase is the address phase. In this phase, an I2C master initiates a write operation to the TVP5150A decoder by generating a start condition (S) followed by the TVP5150A I2C address, in MSB first bit order, followed by a 0 to indicate a write cycle. After receiving acknowledges from the TVP5150A decoder, the master presents the subaddress of the register or the first of a block of registers it wants to read. After the cycle is acknowledged, the master terminates the cycle immediately by generating a stop condition (P).

Table 2−7. Read Address Selection

I2CSEL	READ ADDRESS
0	B9h
1	BBh

The second phase is the data phase. In this phase, an I2C master initiates a read operation to the TVP5150A decoder by generating a start condition followed by the TVP5150A I2C address (as shown below for a read operation), in MSB first bit order, followed by a 1 to indicate a read cycle. After an acknowledge from the TVP5150A decoder, the I2C master receives one or more bytes of data from the TVP5150A decoder. The I2C master acknowledges the transfer at the end of each byte. After the last data byte desired has been transferred from the TVP5150A decoder to the master, the master generates a not acknowledge followed by a stop.

2.15.2.1 Read Phase 1

Step 1	0
I2C Start (master)	S

Step 2	7	6	5	4	3	2	1	0
I2C General address (master)	1	0	1	1	1	0	X	0

Step 3	9
I2C Acknowledge (slave)	A

Step 4	7	6	5	4	3	2	1	0
I2C Read register address (master)	addr	addr	addr	addr	addr	addr	addr	addr

Step 5	9
I2C Acknowledge (slave)	A

Step 6	0
I2C Stop (master)	P

2.15.2.2 Read Phase 2

Step 7	0
I2C Start (master)	S

Step 8	7	6	5	4	3	2	1	0
I2C General address (master)	1	0	1	1	1	0	X	1

Step 9	9
I2C Acknowledge (slave)	A

Step 10	7	6	5	4	3	2	1	0
I2C Read data (slave)	Data	Data	Data	Data	Data	Data	Data	Data

Step 11†	9
I2C Not acknowledge (master)	$\overline{A}$

Step 12	0
I2C Stop (master)	P

† Repeat steps 10 and 11 for all bytes read. Master does not acknowledge the last read data received.

2.15.2.3 I2C Timing Requirements

The TVP5150A decoder requires delays in the I2C accesses to accommodate its internal processor's timing. In accordance with I2C specifications, the TVP5150A decoder holds the I2C clock line (SCL) low to indicate the wait period to the I2C master. If the I2C master is not designed to check for the I2C clock line held-low condition, then the maximum delays must always be inserted where required. These delays are of variable length; maximum delays are indicated in the following diagram:

Normal register writing address 00h−8Fh (addresses 90h−FFh do not require delays)

Start	Slave address (B8h)	Ack	Subaddress	Ack	Data (XXh)	Ack	Wait 64 µs	Stop

The 64-µs delay is for all registers that do not require a reinitialization. Delays may be more for some registers.

2.16 Clock Circuits

An internal line-locked PLL generates the system and pixel clocks. A 14.31818-MHz clock is required to drive the PLL. This may be input to the TVP5150A decoder on terminal 5 (XTAL1), or a crystal of 14.31818-MHz fundamental resonant frequency may be connected across terminals 5 and 6 (XTAL2). Figure 2−5 shows the reference clock configurations. For the example crystal circuit shown (a parallel-resonant crystal with 14.31818-MHz fundamental frequency), the external capacitors must have the following relationship:

$C_{L1} = C_{L2} = 2C_L - C_{STRAY}$,

where C_{STRAY} is the terminal capacitance with respect to ground. Figure 2−5 shows the reference clock configurations.

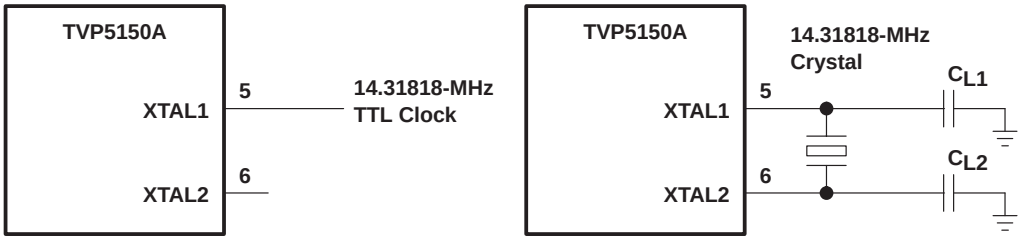


Figure 2−5. Reference Clock Configurations

2.17 Genlock Control and RTC

A Genlock control (GLCO) function is provided to support a standard video encoder to synchronize its internal color oscillator for properly reproduced color with unstable timebase sources like VCRs.

The frequency control word of the internal color subcarrier digital control oscillator (DTO) and the subcarrier phase reset bit are transmitted via terminal 23 (GLCO). The frequency control word is a 23-bit binary number. The frequency of the DTO can be calculated from the following equation:

$$F_{dto} = \frac{F_{ctrl}}{2^{23}} \times F_{sclk}$$

where F_{dto} is the frequency of the DTO, F_{ctrl} is the 23-bit DTO frequency control, and F_{sclk} is the frequency of the SCLK.

2.17.1 TVP5150A Genlock Control Interface

A write of 1 to bit 4 of the chrominance control register at I^2C subaddress 1Ah causes the subcarrier DTO phase reset bit to be sent on the next scan line on GLCO. The active low reset bit occurs 7 SCLKs after the transmission of the last bit of DCO frequency control. Upon the transmission of the reset bit, the phase of the TVP5150A internal subcarrier DCO is reset to zero.

A Genlock slave device can be connected to the GLCO terminal and uses the information on GLCO to synchronize its internal color phase DCO to achieve clean line and color lock.

Figure 2−6 shows the timing diagram of the GLCO mode.

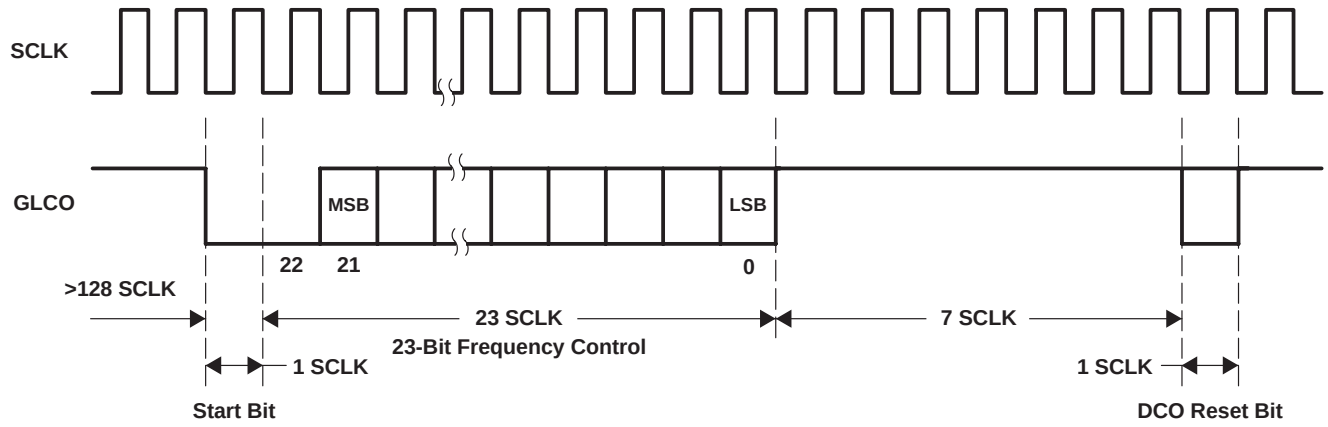


Figure 2−6. GLCO Timing

2.17.2 RTC Mode

Figure 2−7 shows the timing diagram of the RTC mode. Clock rate for the RTC mode is 4 times slower than the GLCO clock rate. For PLL frequency control, the upper 22 bits are used. Each frequency control bit is 2 clock cycles long. The active low reset bit occurs 6 CLKs after the transmission of the last bit of PLL frequency control.

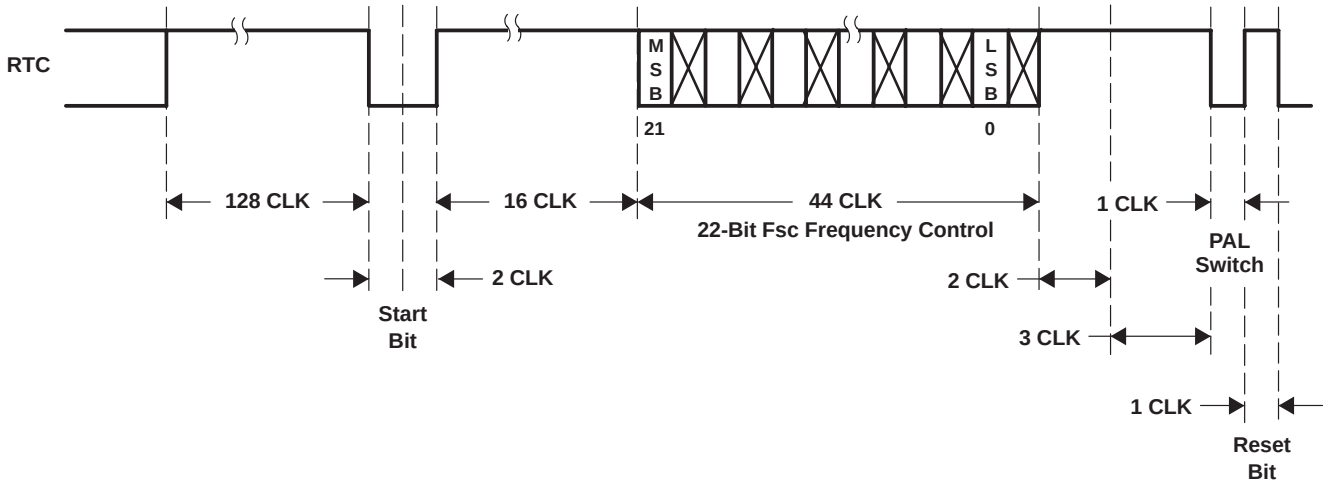


Figure 2−7. RTC Timing

2.18 Reset and Power Down

Terminals 8 (RESETB) and 28 (PDN) work together to put the TVP5150A decoder into one of the two modes. Table 2−8 shows the configuration.

Table 2−8. Reset and Power Down Modes

PDN	RESETB	CONFIGURATION
0	0	Reserved (unknown state)
0	1	Powers down the decoder
1	0	Resets the decoder
1	1	Normal operation

2.19 Internal Control Registers

The TVP5150A decoder is initialized and controlled by a set of internal registers which set all device operating parameters. Communication between the external controller and the TVP5150A decoder is through I^2C. Table 2−9 shows the summary of these registers. The reserved registers must not be written. Reserved bits in the defined registers must be written with 0s, unless otherwise noted. The detailed programming information of each register is described in the following sections.

Table 2−9. Registers Summary

REGISTER FUNCTION	ADDRESS	DEFAULT	R/W
Video input source selection #1	00h	00h	R/W
Analog channel controls	01h	15h	R/W
Operation mode controls	02h	00h	R/W
Miscellaneous controls	03h	01h	R/W
Autoswitch mask:			
TVP5150A	04h	FCh	R/W
TVP5150AM1	04h	DCh	R/W
Reserved	05h	00h	R/W
Color killer threshold control	06h	10h	R/W
Luminance processing control #1	07h	60h	R/W
Luminance processing control #2	08h	00h	R/W
Brightness control	09h	80h	R/W
Color saturation control	0Ah	80h	R/W
Hue control	0Bh	00h	R/W
Contrast control	0Ch	80h	R/W
Outputs and data rates select	0Dh	47h	R/W
Luminance processing control #3	0Eh	00h	R/W
Configuration shared pins	0Fh	08h	R/W
Reserved	10h		
Active video cropping start MSB	11h	00h	R/W
Active video cropping start LSB	12h	00h	R/W
Active video cropping stop MSB	13h	00h	R/W
Active video cropping stop LSB	14h	00h	R/W
Genlock/RTC	15h	01h	R/W
Horizontal sync start	16h	80h	R/W
Reserved	17h		
Vertical blanking start	18h	00h	R/W
Vertical blanking stop	19h	00h	R/W
Chrominance processing control #1	1Ah	0Ch	R/W
Chrominance processing control #2	1Bh	14h	R/W
Interrupt reset register B	1Ch	00h	R/W
Interrupt enable register B	1Dh	00h	R/W
Interrupt configuration register B	1Eh	00h	R/W
Reserved	1Fh−27h		
Video standard	28h	00h	R/W
Reserved	29h−2Bh		
Cb gain factor	2Ch		R
Cr gain factor	2Dh		R
Macrovision on counter	2Eh	0Fh	R/W
Macrovision off counter	2Fh	01h	R/W
656 revision select (TVP5150AM1 only)	30h	00h	R/W

R = Read only
W = Write only
R/W = Read and write

Table 2−9. Registers Summary (Continued)

REGISTER FUNCTION	ADDRESS	DEFAULT	R/W
Reserved	31h−7Fh		
MSB of device ID	80h	51h	R
LSB of device ID	81h	50h	R
ROM major version:			
TVP5150A	82h	03h	R
TVP5150AM1	82h	04h	R
ROM minor version:			
TVP5150A	83h	21h	R
TVP5150AM1	83h	00h	R
Vertical line count MSB	84h		R
Vertical line count LSB	85h		R
Interrupt status register B	86h		R
Interrupt active register B	87h		R
Status register #1	88h		R
Status register #2	89h		R
Status register #3	8Ah		R
Status register #4	8Bh		R
Status register #5	8Ch		R
Reserved	8Dh−8Fh		
Closed caption data registers	90h−93h		R
WSS data registers	94h−99h		R
VPS data registers	9Ah−A6h		R
VITC data registers	A7h−AFh		R
VBI FIFO read data	B0h		R
Teletext filter 1	B1h−B5h	00h	R/W
Teletext filter 2	B6h−BAh	00h	R/W
Teletext filter enable	BBh	00h	R/W
Reserved	BCh−BFh		
Interrupt status register A	C0h	00h	R/W
Interrupt enable register A	C1h	00h	R/W
Interrupt configuration	C2h	04h	R/W
VDP configuration RAM data	C3h	DCh	R/W
Configuration RAM address low byte	C4h	0Fh	R/W
Configuration RAM address high byte	C5h	00h	R/W
VDP status register	C6h		R
FIFO word count	C7h		R
FIFO interrupt threshold	C8h	80h	R/W
FIFO reset	C9h	00h	W
Line number interrupt	CAh	00h	R/W
Pixel alignment register low byte	CBh	4Eh	R/W
Pixel alignment register high byte	CCh	00h	R/W

R = Read only
W = Write only
R/W = Read and write

Table 2−9. Registers Summary (Continued)

REGISTER FUNCTION	ADDRESS	DEFAULT	R/W
FIFO output control	CDh	01h	R/W
Reserved	CEh		
Full field enable	CFh	00h	R/W
Line mode registers	D0h D1h−FBh	00h FFh	R/W
Full field mode register	FCh	7Fh	R/W
Reserved	FDh−FFh		

R = Read only
W = Write only
R/W = Read and write

2.20 Register Definitions

2.20.1 Video Input Source Selection #1 Register

Address	00h
Default	00h

7	6	5	4	3	2	1	0
Reserved				Black output	Reserved	Channel 1 source selection	S-video selection

Channel 1 source selection:

0 = AIP1A selected (default)
1 = AIP1B selected

Table 2−10. Analog Channel and Video Mode Selection

	INPUT(S) SELECTED	ADDRESS 00	
		BIT 1	BIT 0
Composite	AIP1A (default)	0	0
	AIP1B	1	0
S-Video	AIP1A (luma), AIP1B (chroma)	x	1

Black output:

0 = Normal operation (default)
1 = Force black screen output (outputs synchronized)
a. Forced to 10h in normal mode
b. Forced to 01h in extended mode

2.20.2 Analog Channel Controls Register

Address	01h
Default	15h

7	6	5	4	3	2	1	0
Reserved			1	Automatic offset control		Automatic gain control	

Automatic offset control:

00 = Disabled
01 = Automatic offset enabled (default)
10 = Reserved
11 = Offset level frozen to the previously set value

Automatic gain control (AGC):

00 = Disabled (fixed gain value)
01 = AGC enabled (default)
10 = Reserved
11 = AGC frozen to the previously set value

2.20.3 Operation Mode Controls Register

Address	02h
Default	00h

7	6	5	4	3	2	1	0
Reserved	Color burst reference enable	TV/VCR mode		White peak disable	Color subcarrier PLL frozen	Luma peak disable	Power down mode

Color burst reference enable

0 = Color burst reference for AGC disabled (default)
1 = Color burst reference for AGC enabled

TV/VCR mode

00 = Automatic mode determined by the internal detection circuit. (default)
01 = Reserved
10 = VCR (nonstandard video) mode
11 = TV (standard video) mode

With automatic detection enabled, unstable or nonstandard syncs on the input video forces the detector into the VCR mode. This turns off the comb filters and turns on the chroma trap filter.

White peak disable

0 = White peak protection enabled (default)
1 = White peak protection disabled

Color subcarrier PLL frozen:

0 = Color subcarrier PLL increments by the internally generated phase increment. (default)
GLCO pin outputs the frequency increment.
1 = Color subcarrier PLL stops operating.
GLCO pin outputs the frozen frequency increment.

Luma peak disable

0 = Luma peak processing enabled (default)
1 = Luma peak processing disabled

Power down mode:

0 = Normal operation (default)
1 = Power down mode. A/Ds are turned off and internal clocks are reduced to minimum.

2.20.4 Miscellaneous Control Register

Address	03h
Default	01h

7	6	5	4	3	2	1	0
VBKO	GPCL pin	GPCL output enable	Lock status (HVLK)	YCbCr output enable (TVPOE)	HSYNC, VSYNC/PALI, AVID, FID/GLCO output enable	Vertical blanking on/off	Clock output enable

VBKO (pin 27) function select:

0 = GPCL (default)
1 = VBLK

GPCL (data is output based on state of bit 5):

0 = GPCL outputs 0 (default)
1 = GPCL outputs 1

GPCL output enable:

0 = GPCL is inactive (default)
1 = GPCL is output

NOTE: GPCL must not be programmed to be 0 when register 0Fh bit 1 is 1 (GPCL/VBLK).

Lock status (HVLK) (configured along with register 0Fh, please see Figure 2−8 for the relationship between the configuration shared pins):

0 = Terminal VSYNC/PALI outputs the PAL indicator (PALI) signal and terminal FID/GLCO outputs the field ID (FID) signal (default) (if terminals are configured to output PALI and FID in register 0Fh)
1 = Terminal VSYNC/PALI outputs the horizontal lock indicator (HLK) and terminal FID outputs the vertical lock indicator (VLK) (if terminals are configured to output PALI and FID in register 0Fh)

These are additional functionalities that are provided for ease of use.

YCbCr output enable:

0 = YOUT[7:0] high impedance (default)
1 = YOUT[7:0] active

HSYNC, VSYNC/PALI, active video indicator (AVID), and FID/GLCO output enables:

0 = HSYNC, VSYNC/PALI, AVID, and FID/GLCO are high-impedance (default).
1 = HSYNC, VSYNC/PALI, AVID, and FID/GLCO are active.

Vertical blanking on/off:

0 = Vertical blanking (VBLK) off (default)
1 = Vertical blanking (VBLK) on

Clock output enable:

0 = SCLK output is high impedance.
1 = SCLK output is enabled (default).

NOTE: When enabling the outputs, ensure the clock output is not accidently disabled.

Table 2−11. Digital Output Control

Register 03h, Bit 3 (TVPOE)	Register C2h, Bit 2 (VDPOE)	YCbCr Output	Notes
0	X	High impedance	After both YCbCr output enable bits are programmed.
X	0	High impedance	After both YCbCr output enable bits are programmed.
1	1	Active	After both YCbCr output enable bits are programmed.

NOTE: VDPOE default is 1 and TVPOE default is 0.

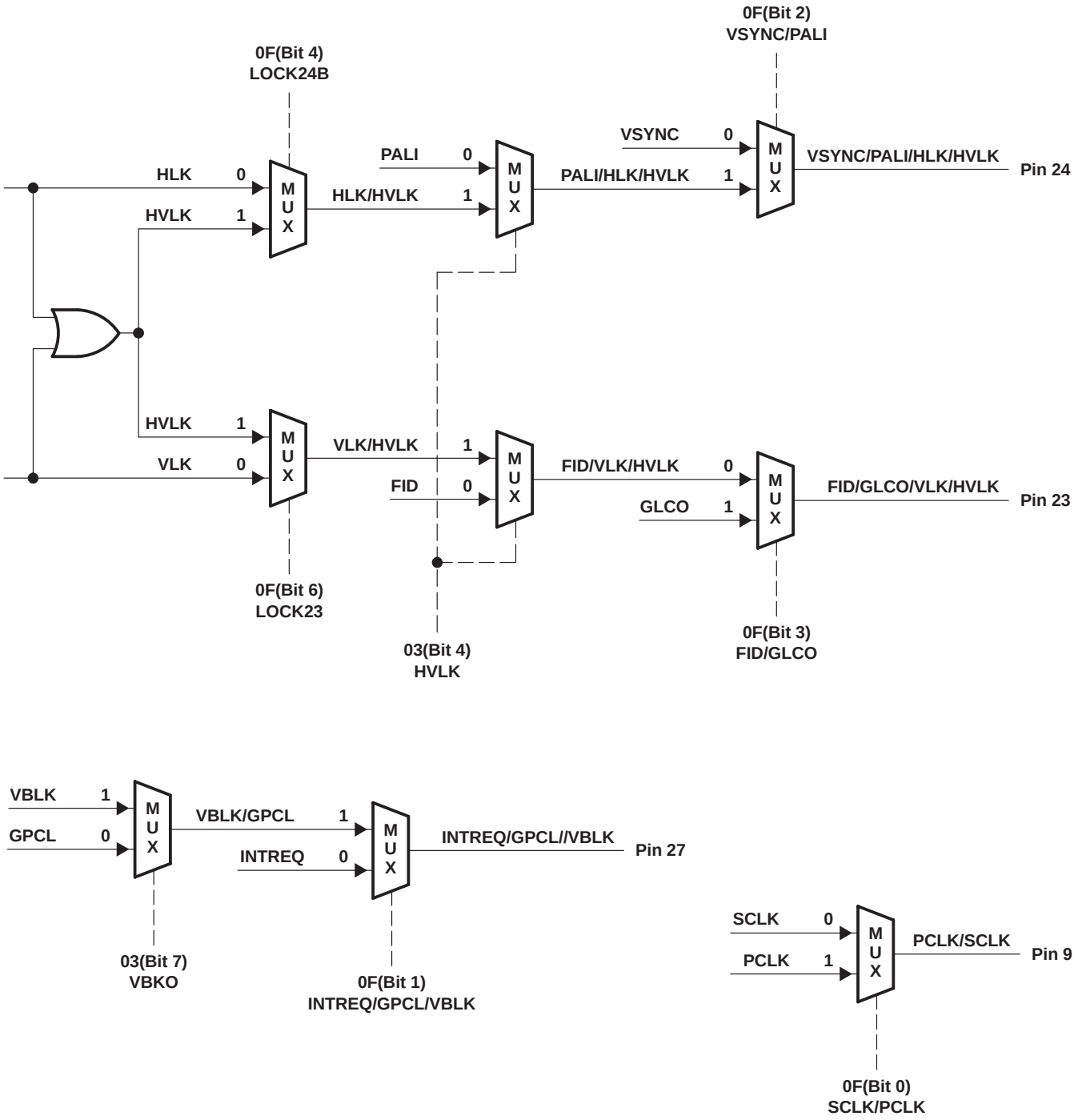


Figure 2−8. Configuration Shared Pins

NOTE: Also refer to the configuration shared pins register at subaddress 0Fh.

2.20.5 Autoswitch Mask Register

Address	04h	
Device	TVP5150A	TVP5150AM1
Default	FCh	DCh

7	6	5	4	3	2	1	0
Reserved		SEC_OFF	N443_OFF	PALN_OFF	PALM_OFF	Reserved	

N443_OFF:

0 = NTSC443 is unmasked from the autoswitch process. Autoswitch does switch to NTSC443.
1 = NTSC443 is masked from the autoswitch process. Autoswitch does not switch to NTSC443. (default)

PALN_OFF:

0 = PAL-N is unmasked from the autoswitch process. Autoswitch does switch to PAL-N.
1 = PAL-N is masked from the autoswitch process. Autoswitch does not switch to PAL-N. (default)

PALM_OFF:

0 = PAL-M is unmasked from the autoswitch process. Autoswitch does switch to PAL-M.
1 = PAL-M is masked from the autoswitch process. Autoswitch does not switch to PAL-M. (default)

SEC_OFF:

0 = SECAM is unmasked from the autoswitch process. Autoswitch does switch to SECAM. (default for TVP5150AM1)
1 = SECAM is masked from the autoswitch process. Autoswitch does not switch to SECAM. (default for TVP5150A)

2.20.6 Color Killer Threshold Control Register

Address	06h
Default	10h

7	6	5	4	3	2	1	0
Reserved	Automatic color killer		Color killer threshold				

Automatic color killer:

00 = Automatic mode (default)
01 = Reserved
10 = Color killer enabled, the CbCr terminals are forced to a zero color state.
11 = Color killer disabled

Color killer threshold:

11111 = −30 dB (minimum)
10000 = −24 dB (default)
00000 = −18 dB (maximum)

2.20.7 Luminance Processing Control #1 Register

Address	07h
Default	60h

7	6	5	4	3	2	1	0
2x luma output enable	Pedestal not present	Disable raw header	Luma bypass enabled during vertical blanking	Luminance signal delay with respect to chrominance signal			

2x luma output enable:

0 = Output depends on bit 4, luminance bypass enabled during vertical blanking (default).
1 = Outputs 2x luma samples during the entire frame. This bit takes precedence over bit 4.

Pedestal not present:

0 = 7.5 IRE pedestal is present on the analog video input signal.
1 = Pedestal is not present on the analog video input signal (default).

Disable raw header:

0 = Insert 656 ancillary headers for raw data
1 = Disable 656 ancillary headers and instead force dummy ones (0x40) (default)

Luminance bypass enabled during vertical blanking:

0 = Disabled. If bit 7, 2x luma output enable, is 0, then normal luminance processing occurs and YCbCr samples are output during the entire frame (default).
1 = Enabled. If bit 7, 2x luma output enable, is 0, then normal luminance processing occurs and YCbCr samples are output during VACTIVE and 2x luma samples are output during VBLK. Luminance bypass occurs for the duration of the vertical blanking as defined by registers 18h and 19h.

Luminance bypass occurs for the duration of the vertical blanking as defined by registers 18h and 19h.

Luma signal delay with respect to chroma signal in pixel clock increments (range −8 to +7 pixel clocks):

1111 = −8 pixel clocks delay
1011 = −4 pixel clocks delay
1000 = −1 pixel clocks delay
0000 = 0 pixel clocks delay (default)
0011 = 3 pixel clocks delay
0111 = 7 pixel clocks delay

2.20.8 Luminance Processing Control #2 Register

Address	08h
Default	00h

7	6	5	4	3	2	1	0
Reserved	Luminance filter select	Reserved		Peaking gain		Mac AGC control	

Luminance filter select:

0 = Luminance comb filter enabled (default)
1 = Luminance chroma trap filter enabled

Peaking gain (sharpness):

00 = 0 (default)
01 = 0.5
10 = 1
11 = 2

Information on peaking frequency: ITU-R BT.601 sampling rate: all standards—peaking center frequency is 2.6 MHz

Mac AGC control:

00 = Auto mode
01 = Auto mode
10 = Force Macrovision AGC pulse detection off
11 = Force Macrovision AGC pulse detection on

2.20.9 Brightness Control Register

Address	09h
Default	80h

7	6	5	4	3	2	1	0
Brightness control							

Brightness control:

1111 1111 = 255 (bright)
1000 0000 = 128 (default)
0000 0000 = 0 (dark)

2.20.10 Color Saturation Control Register

Address	0Ah
Default	80h

7	6	5	4	3	2	1	0
Saturation control							

Saturation control:

1111 1111 = 255 (maximum)
1000 0000 = 128 (default)
0000 0000 = 0 (no color)

2.20.11 Hue Control Register

(does not apply to SECAM)

Address	0Bh
Default	00h

7	6	5	4	3	2	1	0
Hue control							

Hue control:

0111 1111 = +180 degrees
0000 0000 = 0 degrees (default)
1000 0000 = −180 degrees

2.20.12 Contrast Control Register

Address	0Ch
Default	80h

7	6	5	4	3	2	1	0
Contrast control							

Contrast control:

1111 1111 = 255 (maximum contrast)
1000 0000 = 128 (default)
0000 0000 = 0 (minimum contrast)

2.20.13 Outputs and Data Rates Select Register

Address	0Dh
Default	47h

7	6	5	4	3	2	1	0
Reserved	YCbCr output code range	CbCr code format	YCbCr data path bypass		YCbCr output format		

YCbCr output code range:

0 = ITU-R BT.601 coding range (Y ranges from 16 to 235. U and V range from 16 to 240)
1 = Extended coding range (Y, U, and V range from 1 to 254) (default)

CbCr code format:

0 = Offset binary code (2s complement + 128) (default)
1 = Straight binary code (2s complement)

YCbCr data path bypass:

00 = Normal operation (default)
01 = Decimation filter output connects directly to the YCbCr output pins. This data is similar to the digitized composite data, but the HBLANK area is replaced with ITU-R BT.656 digital blanking.
10 = Digitized composite (or digitized S-video luma). A/D output connects directly to the YCbCr output pins.
11 = Reserved

YCbCr output format:

000 = 8-bit 4:2:2 YCbCr with discrete sync output
001 = Reserved
010 = Reserved
011 = Reserved
100 = Reserved
101 = Reserved
110 = Reserved
111 = 8-bit ITU-R BT.656 interface with embedded sync output (default)

2.20.14 Luminance Processing Control #3 Register

Address	0Eh
Default	00h

7	6	5	4	3	2	1	0
Reserved						Luminance trap filter select	

Luminance filter stop band bandwidth (MHz):

00 = No notch (default)
01 = Notch 1
10 = Notch 2
11 = Notch 3

Luminance filter select [1:0] selects one of the four chroma trap (notch) filters to produce luminance signal by removing the chrominance signal from the composite video signal. The stopband of the chroma trap filter is centered at the chroma subcarrier frequency with stopband bandwidth controlled by the two control bits. Please refer to the following table for the stopband bandwidths. The WCF bit is controlled in the chrominance control #2 register, see Section 2.20.25.

WCF	FILTER SELECT	NTSC/PAL/SECAM ITU-R BT.601
0	00	1.2214
	01	0.8782
	10	0.7297
	11	0.4986
1	00	1.4170
	01	1.0303
	10	0.8438
	11	0.5537

2.20.15 Configuration Shared Pins Register

Address	0Fh
Default	08h

7	6	5	4	3	2	1	0
Reserved	LOCK23	Reserved	LOCK24B	FID/GLCO	VSYNC/PALI	INTREQ/GPCL/VBLK	SCLK/PCLK

LOCK23 (pin 23) function select:

0 = FID (default, if bit 3 is selected to output FID)
1 = Lock indicator (indicates whether the device is locked vertically)

LOCK24B (pin 24) function select:

0 = PALI (default, if bit 2 is selected to output PALI)
1 = Lock indicator (indicates whether the device is locked horizontally)

FID/GLCO (pin 23) function select (also refer to register 03h for enhanced functionality):

0 = FID
1 = GLCO (default)

VSYNC/PALI (pin 24) function select (also refer to register 03h for enhanced functionality):

0 = VSYNC (default)
1 = PALI

INTREQ/GPCL/VBLK (pin 27) function select:

0 = INTREQ (default)
1 = GPCL or VBLK depending on bit 7 of register 03h

SCLK/PCLK (pin 9) function select:

0 = SCLK (default)
1 = PCLK (1x pixel clock frequency)

Please see Figure 2−8 for the relationship between the configuration shared pins.

2.20.16 Active Video Cropping Start Pixel MSB Register

Address	11h
Default	00h

7	6	5	4	3	2	1	0
AVID start pixel MSB [7:0]							

Active video cropping start pixel MSB [9:2], set this register first before setting register 12h. The TVP5150A decoder updates the AVID start values only when register 12h is written to. This start pixel value is relative to the default values of the AVID start pixel.

2.20.17 Active Video Cropping Start Pixel LSB Register

Address	12h
Default	00h

7	6	5	4	3	2	1	0
Reserved					AVID active	AVID start pixel LSB [1:0]	

AVID active:

0 = AVID out active in VBLK (default)
1 = AVID out inactive in VBLK

Active video cropping start pixel LSB [1:0]: The TVP5150A decoder updates the AVID start values only when this register is written to.

AVID start [9:0] (combined registers 11h and 12h):

01 1111 1111 = 511
00 0000 0001 = 1
00 0000 0000 = 0 (default)
11 1111 1111 = −1
10 0000 0000 = −512

2.20.18 Active Video Cropping Stop Pixel MSB Register

Address	13h
Default	00h

7	6	5	4	3	2	1	0
AVID stop pixel MSB							

Active video cropping stop pixel MSB [9:2], set this register first before setting the register 14h. The TVP5150A decoder updates the AVID stop values only when register 14h is written to. This stop pixel value is relative to the default values of the AVID stop pixel.

2.20.19 Active Video Cropping Stop Pixel LSB Register

Address	14h
Default	00h

7	6	5	4	3	2	1	0
Reserved						AVID stop pixel LSB	

Active video cropping stop pixel LSB [1:0]: The number of pixels of active video must be an even number. The TVP5150A decoder updates the AVID stop values only when this register is written to.

AVID stop [9:0] (combined registers 13h and 14h):

01 1111 1111 = 511
00 0000 0001 = 1
00 0000 0000 = 0 (default) (see Figure 2−3 and Figure 2−4)
11 1111 1111 = −1
10 0000 0000 = −512

2.20.20 Genlock and RTC Register

Address	15h
Default	01h

7	6	5	4	3	2	1	0
Reserved		F/V bit control		Reserved	GLCO/RTC		

F/V bit control

BIT 5	BIT 4	NUMBER OF LINES	F BIT	V BIT
0	0	Standard	ITU-R BT.656	ITU-R BT.656
		Nonstandard even	Force to 1	Switch at field boundary
		Nonstandard odd	Toggles	Switch at field boundary
0	1	Standard	ITU-R BT.656	ITU-R BT.656
		Nonstandard	Toggles	Switch at field boundary
1	0	Standard	ITU-R BT.656	ITU-R BT.656
		Nonstandard	Pulse mode	Switch at field boundary
1	1	Illegal		

GLCO/RTC. The following table helps in understanding the different modes.

BIT 2	BIT 1	BIT 0	GENLOCK/RTC MODE
0	X	0	GLCO
0	X	1	RTC output mode 0 (default)
1	X	0	GLCO
1	X	1	RTC output mode 1

All other values are reserved.

Figure 2−6 shows the timing of GLCO and Figure 2−7 shows the timing of RTC.

2.20.21 Horizontal Sync (HSYNC) Start Register

Address	16h
Default	80h

7	6	5	4	3	2	1	0
HSYNC start							

HSYNC start:

1111 1111 = −127 x 4 pixel clocks
1111 1110 = −126 x 4 pixel clocks
1000 0001 = −1 x 4 pixel clocks
1000 0000 = 0 pixel clocks (default)
0111 1111 = 1 x 4 pixel clocks
0111 1110 = 2 x 4 pixel clocks
0000 0000 = 128 x 4 pixel clocks

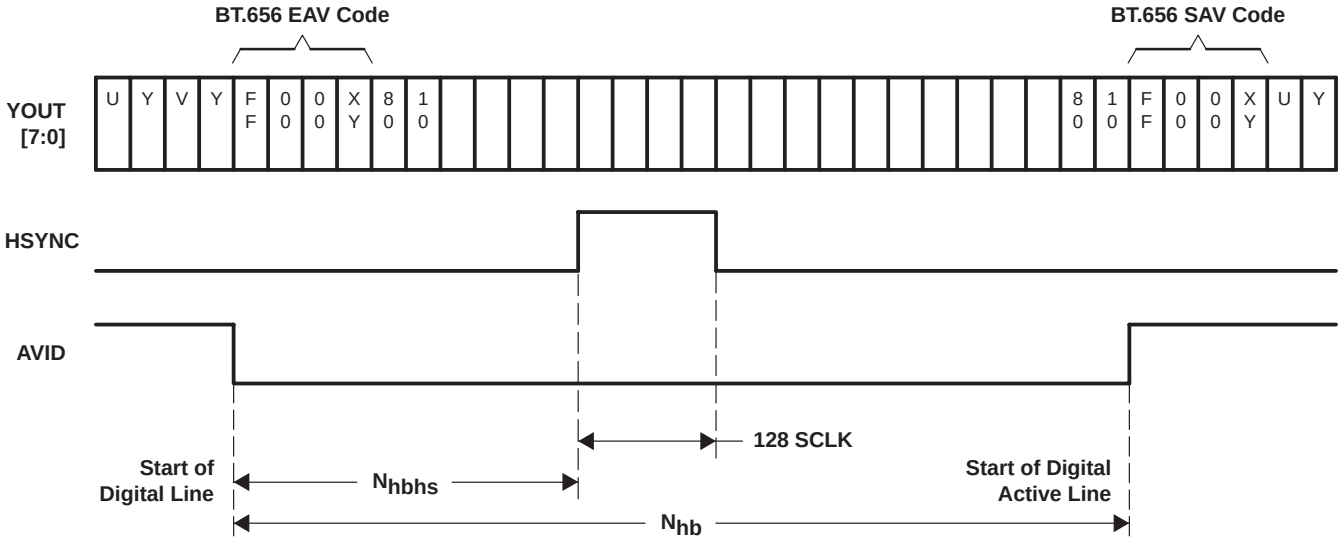


Figure 2−9. Horizontal Sync

Table 2−12. Clock Delays (SCLKs)

STANDARD	N_{hbhs}	N_{hb}
NTSC	16	272
PAL	20	284
SECAM	40	280

Detailed timing information is also available in Section 2.12, *Synchronization Signals*.

2.20.22 Vertical Blanking Start Register

Address	18h
Default	00h

7	6	5	4	3	2	1	0
Vertical blanking start							

Vertical blanking (VBLK) start:

0111 1111 = 127 lines after start of vertical blanking interval
0000 0001 = 1 line after start of vertical blanking interval
0000 0000 = Same time as start of vertical blanking interval (default) (see Figure 2−2)
1111 1111 = 1 line before start of vertical blanking interval
1000 0000 = 128 lines before start of vertical blanking interval

Vertical blanking is adjustable with respect to the standard vertical blanking intervals. The setting in this register determines the timing of the GPCL/VBLK signal when it is configured to output vertical blank (see register 03h). The setting in this register also determines the duration of the luma bypass function (see register 07h).

2.20.23 Vertical Blanking Stop Register

Address	19h
Default	00h

7	6	5	4	3	2	1	0
Vertical blanking stop							

Vertical blanking (VBLK) stop:

0111 1111 = 127 lines after stop of vertical blanking interval
0000 0001 = 1 line after stop of vertical blanking interval
0000 0000 = Same time as stop of vertical blanking interval (default) (see Figure 2−2)
1111 1111 = 1 line before stop of vertical blanking interval
1000 0000 = 128 lines before stop of vertical blanking interval

Vertical blanking is adjustable with respect to the standard vertical blanking intervals. The setting in this register determines the timing of the GPCL/VBLK signal when it is configured to output vertical blank (see register 03h). The setting in this register also determines the duration of the luma bypass function (see register 07h).

2.20.24 Chrominance Control #1 Register

Address	1Ah
Default	0Ch

7	6	5	4	3	2	1	0
Reserved			Color PLL reset	Chrominance adaptive comb filter enable (ACE)	Chrominance comb filter enable (CE)	Automatic color gain control	

Color PLL reset:

0 = Color PLL not reset (default)
1 = Color PLL reset

Color PLL phase is reset to zero and the color PLL reset bit then immediately returns to zero. When this bit is set, the subcarrier PLL phase reset bit is transmitted on terminal 23 (GLCO) on the next line (NTSC or PAL).

Chrominance adaptive comb filter enable (ACE):

0 = Disable
1 = Enable (default)

Chrominance comb filter enable (CE):

0 = Disable
1 = Enable (default)

Automatic color gain control (ACGC):

00 = ACGC enabled (default)
01 = Reserved
10 = ACGC disabled
11 = ACGC frozen to the previously set value

2.20.25 Chrominance Control #2 Register

Address	1Bh
Default	14h

7	6	5	4	3	2	1	0
Reserved				Reserved	WCF	Chrominance filter select	

Wideband chroma filter (WCF):

0 = Disable
1 = Enable (default)

Chrominance filter select:

00 = No notch (default)
01 = Notch 1
10 = Notch 2
11 = Notch 3

Chrominance output bandwidth (MHz):

WCF	FILTER SELECT	NTSC/PAL/SECAM ITU-R BT.601
0	00	1.2214
	01	0.8782
	10	0.7297
	11	0.4986
1	00	1.4170
	01	1.0303
	10	0.8438
	11	0.5537

2.20.26 Interrupt Reset Register B

Address	1Ch
Default	00h

7	6	5	4	3	2	1	0
Software initialization reset	Macrovision detect changed reset	Reserved	Field rate changed reset	Line alternation changed reset	Color lock changed reset	H/V lock changed reset	TV/VCR changed reset

Interrupt reset register B is used by the external processor to reset the interrupt status bits in interrupt status register B. Bits loaded with a 1 allow the corresponding interrupt status bit to reset to 0. Bits loaded with a 0 have no effect on the interrupt status bits.

Software initialization reset:

0 = No effect (default)
1 = Reset software initialization bit

Macrovision detect changed reset:

0 = No effect (default)
1 = Reset Macrovision detect changed bit

Field rate changed reset:

0 = No effect (default)
1 = Reset field rate changed bit

Line alternation changed reset:

0 = No effect (default)
1 = Reset line alternation changed bit

Color lock changed reset:

0 = No effect (default)
1 = Reset color lock changed bit

H/V lock changed reset:

0 = No effect (default)
1 = Reset H/V lock changed bit

TV/VCR changed reset [TV/VCR mode is determined by counting the total number of lines/frame. The mode switches to VCR for nonstandard number of lines]:

0 = No effect (default)
1 = Reset TV/VCR changed bit

2.20.27 Interrupt Enable Register B

Address	1Dh
Default	00h

7	6	5	4	3	2	1	0
Software initialization occurred enable	Macrovision detect changed	Reserved	Field rate changed	Line alternation changed	Color lock changed	H/V lock changed	TV/VCR changed

Interrupt enable register B is used by the external processor to mask unnecessary interrupt sources for interrupt B. Bits loaded with a 1 allow the corresponding interrupt condition to generate an interrupt on the external pin. Conversely, bits loaded with 0s mask the corresponding interrupt condition from generating an interrupt on the external pin. This register only affects the external pin, it does not affect the bits in the interrupt status register. A given condition can set the appropriate bit in the status register and not cause an interrupt on the external pin. To determine if this device is driving the interrupt pin either AND interrupt status register B with interrupt enable register B or check the state of interrupt B in the interrupt B active register.

Software initialization occurred enable:

0 = Disabled (default)
1 = Enabled

Macrovision detect changed:

0 = Disabled (default)
1 = Enabled

Field rate changed:

0 = Disabled (default)
1 = Enabled

Line alternation changed:

0 = Disabled (default)
1 = Enabled

Color lock changed:

0 = Disabled (default)
1 = Enabled

H/V lock changed:

0 = Disabled (default)
1 = Enabled

TV/VCR changed:

0 = Disabled (default)
1 = Enabled

2.20.28 Interrupt Configuration Register B

Address	1Eh
Default	00h

7	6	5	4	3	2	1	0
Reserved							Interrupt polarity B

Interrupt polarity B:

0 = Interrupt B is active low (default).
1 = Interrupt B is active high.

Interrupt polarity B must be same as interrupt polarity A bit at bit 0 of the interrupt configuration register A at address C2h.

Interrupt configuration register B is used to configure the polarity of interrupt B on the external interrupt pin. When the interrupt B is configured for active low, the pin is driven low when active and high-impedance when inactive (open-drain). Conversely, when the interrupt B is configured for active high, it is driven high for active and driven low for inactive.

2.20.29 Video Standard Register

Address	28h
Default	00h

7	6	5	4	3	2	1	0
Reserved				Video standard			

Video standard:

0000 = Autoswitch mode (default)
0001 = Reserved
0010 = (M) NTSC ITU-R BT.601
0011 = Reserved
0100 = (B, G, H, I, N) PAL ITU-R BT.601
0101 = Reserved
0110 = (M) PAL ITU-R BT.601
0111 = Reserved
1000 = (Combination-N) PAL ITU-R BT.601
1001 = Reserved
1010 = NTSC 4.43 ITU-R BT.601
1011 = Reserved
1100 = SECAM ITU-R BT.601

With the autoswitch code running, the user can force the device to operate in a particular video standard mode and sample rate by writing the appropriate value into this register.

2.20.30 Cb Gain Factor Register

Address	2Ch

7	6	5	4	3	2	1	0
Cb gain factor							

This is a read-only register that provides the gain applied to the Cb in the YCbCr data stream.

2.20.31 Cr Gain Factor Register

Address	2Dh

7	6	5	4	3	2	1	0
Cr gain factor							

This is a read-only register that provides the gain applied to the Cr in the YCbCr data stream.

2.20.32 Macrovision On Counter Register

Address	2Eh
Default	0Fh

7	6	5	4	3	2	1	0
Macrovision on counter							

This register allows the user to determine how many consecutive frames in which the Macrovision AGC pulses have to be detected before the decoder decides that the Macrovision AGC pulses are present.

2.20.33 Macrovision Off Counter Register

Address	2Fh
Default	01h

7	6	5	4	3	2	1	0
Macrovision off counter							

This register allows the user to determine how many consecutive frames in which the Macrovision AGC pulses are not detected before the decoder decides that the Macrovision AGC pulses are not present.

2.20.34 656 Revision Select Register

NOTE: This register exists only for the TVP5150AM1.

Address	30h
Default	00h

7	6	5	4	3	2	1	0
Reserved							656 revision select

656 revision select:

0 = Adheres to ITU-R BT.656.4 timing (default for TVP5150AM1, this is the only option for TVP5150A).
1 = Adheres to ITU-R BT.656.3 timing.

2.20.35 MSB of Device ID Register

Address	80h
Default	51h

7	6	5	4	3	2	1	0
MSB of device ID							

This register identifies the MSB of the device ID. Value = 0x51.

2.20.36 LSB of Device ID Register

Address	81h
Default	50h

7	6	5	4	3	2	1	0
LSB of device ID							

This register identifies the LSB of the device ID. Value = 0x50.

2.20.37 ROM Major Version Register

Address	82h	
Device	TVP5150A	TVP5150AM1
Default	03h	04h

7	6	5	4	3	2	1	0
ROM major version†							

† This register can contain a number from 0x01 to 0xFF.

Value = 0x03 for TVP5150A
Value = 0x04 for TVP5150AM1

2.20.38 ROM Minor Version Register

Address	83h	
Device	TVP5150A	TVP5150AM1
Default	21h	00h

7	6	5	4	3	2	1	0
ROM minor version†							

† This register can contain a number from 0x01 to 0xFF.

Value = 0x21 for TVP5150A
Value = 0x00 for TVP5150AM1

2.20.39 Vertical Line Count MSB Register

Address	84h

7	6	5	4	3	2	1	0
Reserved						Vertical line count MSB	

Vertical line count bits [9:8]

2.20.40 Vertical Line Count LSB Register

Address	85h

7	6	5	4	3	2	1	0
Vertical line count LSB							

Vertical line count bits [7:0]

Registers 84h and 85h can be read and combined to extract the detected number of lines per frame. This can be used with nonstandard video signals such as a VCR in fast-forward or rewind modes to synchronize the downstream video circuitry.

2.20.41 Interrupt Status Register B

Address	86h

7	6	5	4	3	2	1	0
Software initialization	Macrovision detect changed	Command ready	Field rate changed	Line alternation changed	Color lock changed	H/V lock changed	TV/VCR changed

Software initialization:

0 = Software initialization is not ready (default).
1 = Software initialization is ready.

Macrovision detect changed:

0 = Macrovision detect status has not changed (default).
1 = Macrovision detect status has changed.

Command ready:

0 = TVP5150A is not ready to accept a new command (default).
1 = TVP5150A is ready to accept a new command.

Field rate changed:

0 = Field rate has not changed (default).
1 = Field rate has changed.

Line alternation changed:

0 = Line alteration has not changed (default).
1 = Line alternation has changed.

Color lock changed:

0 = Color lock status has not changed (default).
1 = Color lock status has changed.

H/V lock changed:

0 = H/V lock status has not changed (default).
1 = H/V lock status has changed.

TV/VCR changed:

0 = TV/VCR status has not changed (default).
1 = TV/VCR status has changed.

Interrupt status register B is polled by the external processor to determine the interrupt source for interrupt B. After an interrupt condition is set, it can be reset by writing to the interrupt reset register B at subaddress 1Ch with a 1 in the appropriate bit.

2.20.42 Interrupt Active Register B

Address	87h

7	6	5	4	3	2	1	0
Reserved							Interrupt B

Interrupt B:

0 = Interrupt B is not active on the external terminal (default).
1 = Interrupt B is active on the external terminal.

The interrupt active register B is polled by the external processor to determine if interrupt B is active.

2.20.43 Status Register #1

Address	88h

7	6	5	4	3	2	1	0
Peak white detect status	Line-alternating status	Field rate status	Lost lock detect	Color subcarrier lock status	Vertical sync lock status	Horizontal sync lock status	TV/VCR status

Peak white detect status:

0 = Peak white is not detected.
1 = Peak white is detected.

Line-alternating status:

0 = Nonline alternating
1 = Line alternating

Field rate status:

0 = 60 Hz
1 = 50 Hz

Lost lock detect:

0 = No lost lock since status register #1 was last read.
1 = Lost lock since status register #1 was last read.

Color subcarrier lock status:

0 = Color subcarrier is not locked.
1 = Color subcarrier is locked.

Vertical sync lock status:

0 = Vertical sync is not locked.
1 = Vertical sync is locked.

Horizontal sync lock status:

0 = Horizontal sync is not locked.
1 = Horizontal sync is locked.

TV/VCR status. TV mode is determined by detecting standard line-to-line variations and specific chroma SCH phases based on the standard input video format. VCR mode is determined by detecting variations in the chroma SCH phases compared to the chroma SCH phases of the standard input video format.

0 = TV
1 = VCR

2.20.44 Status Register #2

Address	89h

7	6	5	4	3	2	1	0
Reserved	Weak signal detection	PAL switch polarity	Field sequence status	AGC and offset frozen status	Macrovision detection		

Weak signal detection:

0 = No weak signal
1 = Weak signal mode

PAL switch polarity of first line of odd field:

0 = PAL switch is 0
1 = PAL switch is 1

Field sequence status:

0 = Even field
1 = Odd field

AGC and offset frozen status:

0 = AGC and offset are not frozen.
1 = AGC and offset are frozen.

Macrovision detection:

000 = No copy protection
001 = AGC process present (Macrovision Type 1 present)
010 = Colorstripe process Type 2 present
011 = AGC process and colorstripe process Type 2 present
100 = Reserved
101 = Reserved
110 = Colorstripe process Type 3 present
111 = AGC process and color stripe process Type 3 present

2.20.45 Status Register #3

Address	8Ah

7	6	5	4	3	2	1	0
Front-end AGC gain value (analog and digital)†							

† Represents 8 bits (MSB) of a 10-bit value

This register provides the front-end AGC gain value of both analog and digital gains.

2.20.46 Status Register #4

Address	8Bh

7	6	5	4	3	2	1	0
Subcarrier to horizontal (SCH) phase							

SCH (color PLL subcarrier phase at 50% of the falling edge of horizontal sync of line one of odd field; step size 360°/256):

0000 0000 = 0.00°
0000 0001 = 1.41°
0000 0010 = 2.81°
1111 1110 = 357.2°
1111 1111 = 358.6°

2.20.47 Status Register #5

Address	8Ch

7	6	5	4	3	2	1	0
Autoswitch mode	Reserved			Video standard			Sampling rate

This register contains information about the detected video standard and the sampling rate at which the device is currently operating. When autoswitch code is running, this register must be tested to determine which video standard has been detected.

Autoswitch mode:

0 = Stand-alone (forced video standard) mode
1 = Autoswitch mode

Video standard:

VIDEO STANDARD [3:1]			SR	VIDEO STANDARD
BIT 3	BIT2	BIT1	BIT 0	
0	0	0	0	Reserved
0	0	0	1	(M) NTSC ITU-R BT.601
0	0	1	0	Reserved
0	0	1	1	(B, G, H, I, N) PAL ITU-R BT.601
0	1	0	0	Reserved
0	1	0	1	(M) PAL ITU-R BT.601
0	1	1	0	Reserved
0	1	1	1	PAL-N ITU-R BT.601
1	0	0	0	Reserved
1	0	0	1	NTSC 4.43 ITU-R BT.601
1	0	1	0	Reserved
1	0	1	1	SECAM ITU-R BT.601

Sampling rate (SR):

0 = Reserved
1 = ITU-R BT.601

2.20.48 Closed Caption Data Registers

Address	90h−93h

Address	7	6	5	4	3	2	1	0
90h	Closed caption field 1 byte 1							
91h	Closed caption field 1 byte 2							
92h	Closed caption field 2 byte 1							
93h	Closed caption field 2 byte 2							

These registers contain the closed caption data arranged in bytes per field.

2.20.49 WSS Data Registers

Address	94h−99h

NTSC

ADDRESS	7	6	5	4	3	2	1	0	BYTE
94h			b5	b4	b3	b2	b1	b0	WSS field 1 byte 1
95h	b13	b12	b11	b10	b9	b8	b7	b6	WSS field 1 byte 2
96h			b19	b18	b17	b16	b15	b14	WSS field 1 byte 3
97h			b5	b4	b3	b2	b1	b0	WSS field 2 byte 1
98h	b13	b12	b11	b10	b9	b8	b7	b6	WSS field 2 byte 2
99h			b19	b18	b17	b16	b15	b14	WSS field 2 byte 3

These registers contain the wide screen signaling (WSS) data for NTSC.

Bits 0−1 represent word 0, aspect ratio
Bits 2−5 represent word 1, header code for word 2
Bits 6−13 represent word 2, copy control
Bits 14−19 represent word 3, CRC

PAL/SECAM

ADDRESS	7	6	5	4	3	2	1	0	BYTE
94h	b7	b6	b5	b4	b3	b2	b1	b0	WSS field 1 byte 1
95h			b13	b12	b11	b10	b9	b8	WSS field 1 byte 2
96h	Reserved								
97h	b7	b6	b5	b4	b3	b2	b1	b0	WSS field 2 byte 1
98h			b13	b12	b11	b10	b9	b8	WSS field 2 byte 2
99h	Reserved								

PAL/SECAM:

Bits 0−3 represent group 1, aspect ratio
Bits 4−7 represent group 2, enhanced services
Bits 8−10 represent group 3, subtitles
Bits 11−13 represent group 4, others

2.20.50 VPS Data Registers

Address	9Ah–A6h

ADDRESS	7	6	5	4	3	2	1	0
9Ah	VPS byte 1							
9Bh	VPS byte 2							
9Ch	VPS byte 3							
9Dh	VPS byte 4							
9Eh	VPS byte 5							
9Fh	VPS byte 6							
A0h	VPS byte 7							
A1h	VPS byte 8							
A2h	VPS byte 9							
A3h	VPS byte 10							
A4h	VPS byte 11							
A5h	VPS byte 12							
A6h	VPS byte 13							

These registers contain the entire VPS data line except the clock run-in code or the start code.

2.20.51 VITC Data Registers

Address	A7h–AFh

ADDRESS	7	6	5	4	3	2	1	0
A7h	VITC byte 1, frame byte 1							
A8h	VITC byte 2, frame byte 2							
A9h	VITC byte 3, seconds byte 1							
AAh	VITC byte 4, seconds byte 2							
ABh	VITC byte 5, minutes byte 1							
ACh	VITC byte 6, minutes byte 2							
ADh	VITC byte 7, hour byte 1							
AEh	VITC byte 8, hour byte 2							
AFh	VITC byte 9, CRC							

These registers contain the VITC data.

2.20.52 VBI FIFO Read Data Register

Address	B0h

7	6	5	4	3	2	1	0
FIFO read data							

This address is provided to access VBI data in the FIFO through the host port. All forms of teletext data come directly from the FIFO, while all other forms of VBI data can be programmed to come from the registers or from the FIFO. Current status of the FIFO can be found at address C6h and the number of bytes in the FIFO is located at address C7h. If the host port is to be used to read data from the FIFO, then the output formatter must be disabled at address CDh bit 0. The format used for the VBI FIFO is shown in Section 2.9.

2.20.53 Teletext Filter and Mask Registers

Address	B1h–BAh
Default	00h

ADDRESS	7	6	5	4	3	2	1	0
B1h	Filter 1 mask 1				Filter 1 pattern 1			
B2h	Filter 1 mask 2				Filter 1 pattern 2			
B3h	Filter 1 mask 3				Filter 1 pattern 3			
B4h	Filter 1 mask 4				Filter 1 pattern 4			
B5h	Filter 1 mask 5				Filter 1 pattern 5			
B6h	Filter 2 mask 1				Filter 2 pattern 1			
B7h	Filter 2 mask 2				Filter 2 pattern 2			
B8h	Filter 2 mask 3				Filter 2 pattern 3			
B9h	Filter 2 mask 4				Filter 2 pattern 4			
BAh	Filter 2 mask 5				Filter 2 pattern 5			

For an NABTS system, the packet prefix consists of five bytes. Each byte contains four data bits (D[3:0]) interlaced with four Hamming protection bits (H[3:0]):

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D[3]	H[3]	D[2]	H[2]	D[1]	H[1]	D[0]	H[0]

Only the data portion D[3:0] from each byte is applied to a teletext filter function with the corresponding pattern bits P[3:0] and mask bits M[3:0]. Hamming protection bits are ignored by the filter.

For a WST system (PAL or NTSC), the packet prefix consists of two bytes so that two patterns are used. Patterns 3, 4, and 5 are ignored.

The mask bits enable filtering using the corresponding bit in the pattern register. For example, a 1 in the LSB of mask 1 means that the filter module must compare the LSB of nibble 1 in the pattern register to the first data bit on the transaction. If these match, then a true result is returned. A 0 in a bit of mask 1 means that the filter module must ignore that data bit of the transaction. If all 0s are programmed in the mask bits, then the filter matches all patterns returning a true result (default 00h).

Pattern and mask for each byte and filter are referred as <1,2><P,M><1,2,3,4,5> where:

<1,2> identifies the filter 1 or 2
<P,M> identifies the pattern or mask
<1,2,3,4,5> identifies the byte number

2.20.54 Teletext Filter Control Register

Address	BBh
Default	00h

7	6	5	4	3	2	1	0
Reserved			Filter logic		Mode	TTX filter 2 enable	TTX filter 1 enable

Filter logic: allows different logic to be applied when combining the decision of filter 1 and filter 2 as follows:

00 = NOR (Default)
01 = NAND
10 = OR
11 = AND

Mode:

0 = Teletext WST PAL mode B (2 header bytes) (default)
1 = Teletext NABTS NTSC mode C (5 header bytes)

TTX filter 2 enable:

0 = Disabled (default)
1 = Enabled

TTX filter 1 enable:

0 = Disabled (default)
1 = Enabled

If the filter matches or if the filter mask is all 0s, then a true result is returned.

2.20.55 Interrupt Status Register A

Address	C0h
Default	00h

7	6	5	4	3	2	1	0
Lock state interrupt	Lock interrupt	Reserved			FIFO threshold interrupt	Line interrupt	Data interrupt

The interrupt status register A can be polled by the host processor to determine the source of an interrupt. After an interrupt condition is set it can be reset by writing to this register with a 1 in the appropriate bit(s).

Lock state interrupt:

0 = TVP5150A is not locked to the video signal (default).
1 = TVP5150A is locked to the video signal.

Lock interrupt:

0 = A transition has not occurred on the lock signal (default).
1 = A transition has occurred on the lock signal.

FIFO threshold interrupt:

0 = The amount of data in the FIFO has not yet crossed the threshold programmed at address C8h (default).
1 = The amount of data in the FIFO has crossed the threshold programmed at address C8h.

Line interrupt:

0 = The video line number has not yet been reached (default).
1 = The video line number programmed in address CAh has occurred.

Data interrupt:

0 = No data is available (default).
1 = VBI data is available either in the FIFO or in the VBI data registers.

2.20.56 Interrupt Enable Register A

Address	C1h
Default	00h

7	6	5	4	3	2	1	0
Reserved	Lock interrupt enable	Cycle complete interrupt enable	Bus error interrupt enable	Reserved	FIFO threshold interrupt enable	Line interrupt enable	Data interrupt enable

The interrupt enable register A is used by the host processor to mask unnecessary interrupt sources. Bits loaded with a 1 allow the corresponding interrupt condition to generate an interrupt on the external pin. Conversely, bits loaded with a 0 mask the corresponding interrupt condition from generating an interrupt on the external pin. This register only affects the interrupt on the external terminal, it does not affect the bits in interrupt status register A. A given condition can set the appropriate bit in the status register and not cause an interrupt on the external terminal. To determine if this device is driving the interrupt terminal either perform a logical AND of interrupt status register A with interrupt enable register A, or check the state of the interrupt A bit in the interrupt configuration register at address C2h.

Lock interrupt enable:

0 = Disabled (default)
1 = Enabled

Cycle complete interrupt enable:

0 = Disabled (default)
1 = Enabled

Bus error interrupt enable:

0 = Disabled (default)
1 = Enabled

FIFO threshold interrupt enable:

0 = Disabled (default)
1 = Enabled

Line interrupt enable:

0 = Disabled (default)
1 = Enabled

Data interrupt enable:

0 = Disabled (default)
1 = Enabled

2.20.57 Interrupt Configuration Register A

Address	C2h
Default	04h

7	6	5	4	3	2	1	0
Reserved					YCbCr enable (VDPOE)	Interrupt A	Interrupt polarity A

YCbCr enable (VDPOE):

0 = YCbCr pins are high impedance.
1 = YCbCr pins are active if other conditions are met (default).

Interrupt A (read-only):

0 = Interrupt A is not active on the external pin (default).
1 = Interrupt A is active on the external pin.

Interrupt polarity A:

0 = Interrupt A is active low (default).
1 = Interrupt A is active high.

Interrupt configuration register A is used to configure the polarity of the external interrupt terminal. When interrupt A is configured as active low, the terminal is driven low when active and high-impedance when inactive (open collector). Conversely, when the terminal is configured as active high, it is driven high when active and driven low when inactive.

2.20.58 VDP Configuration RAM Register

Address	C3h	C4h	C5h
Default	DCh	0Fh	00h

Address	7	6	5	4	3	2	1	0
C3h	Configuration data							
C4h	RAM address (7:0)							
C5h	Reserved							RAM address 8

The configuration RAM data is provided to initialize the VDP with initial constants. The configuration RAM is 512 bytes organized as 32 different configurations of 16 bytes each. The first 12 configurations are defined for the current VBI standards. An additional 2 configurations can be used as a custom programmed mode for unique standards like Gemstar.

Address C3h is used to read or write to the RAM. The RAM internal address counter is automatically incremented with each transaction. Addresses C5h and C4h make up a 9-bit address to load the internal address counter with a specific start address. This can be used to write a subset of the RAM for only those standards of interest. Registers D0h−FBh must all be programmed with FFh, before writing or reading the configuration RAM. Full field mode (CFh) must be disabled as well.

The suggested RAM contents are shown below. All values are hexadecimal.

Table 2−13. VBI Configuration RAM For Signals With Pedestal

Index	Address	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Reserved	000	Reserved															
WST SECAM 6	010	AA	AA	FF	FF	E7	2E	20	26	e6	b4	0e	0	0	0	10	0
Reserved	020	Reserved															
WST PAL B 6	030	AA	AA	FF	FF	27	2E	20	2B	A6	72	10	0	0	0	10	0
Reserved	040	Reserved															
WST PAL C 6	050	AA	AA	FF	FF	E7	2E	20	22	A6	98	0D	0	0	0	10	0
Reserved	060	Reserved															
WST NTSC 6	070	AA	AA	FF	FF	27	2E	20	23	69	93	0D	0	0	0	10	0
Reserved	080	Reserved															
NABTS, NTSC 6	090	AA	AA	FF	FF	E7	2E	20	22	69	93	0D	0	0	0	15	0
Reserved	0A0	Reserved															
NABTS, NTSC-J 6	0B0	AA	AA	FF	FF	A7	2E	20	23	69	93	0D	0	0	0	10	0
Reserved	0C0	Reserved															
CC, PAL/SECAM 6	0D0	AA	2A	FF	3F	04	51	6E	02	A6	7B	09	0	0	0	27	0
Reserved	0E0	Reserved															
CC, NTSC 6	0F0	AA	2A	FF	3F	04	51	6E	02	69	8C	09	0	0	0	27	0
Reserved	100	Reserved															
WSS, PAL/SECAM 6	110	5B	55	C5	FF	0	71	6E	42	A6	CD	0F	0	0	0	3A	0
Reserved	120	Reserved															
WSS, NTSC C	130	38	00	3F	00	0	71	6E	43	69	7C	08	0	0	0	39	0
Reserved	140	Reserved															
VITC, PAL/SECAM 6	150	0	0	0	0	0	8F	6D	49	A6	85	08	0	0	0	4C	0
Reserved	160	Reserved															
VITC, NTSC 6	170	0	0	0	0	0	8F	6D	49	69	94	08	0	0	0	4C	0
Reserved	180	Reserved															
VPS, PAL 6	190	AA	AA	FF	FF	BA	CE	2B	0D	A6	DA	0B	0	0	0	60	0
Reserved	1A0	Reserved															
Custom 1	1B0	Programmable															
Reserved	1C0	Reserved															
Custom 2	1D0	Programmable															

2.20.59 VDP Status Register

Address	C6h

7	6	5	4	3	2	1	0
FIFO full error	FIFO empty	TTX available	CC field 1 available	CC field 2 available	WSS available	VPS available	VITC available

The VDP status register indicates whether data is available in either the FIFO or data registers, and status information about the FIFO. Reading data from the corresponding register does not clear the status flags automatically. These flags are only reset by writing a 1 to the respective bit. However, bit 6 is updated automatically.

FIFO full error:

0 = No FIFO full error
1 = FIFO was full during a write to FIFO.

The FIFO full error flag is set when the current line of VBI data can not enter the FIFO. For example, if the FIFO has only 10 bytes left and teletext is the current VBI line, the FIFO full error flag is set, but no data is written because the entire teletext line will not fit. However, if the next VBI line is closed caption requiring only 2 bytes of data plus the header, this goes into the FIFO. Even if the full error flag is set.

FIFO empty:

0 = FIFO is not empty.
1 = FIFO is empty.

TTX available:

0 = Teletext data is not available.
1 = Teletext data is available.

CC field 1 available:

0 = Closed caption data from field 1 is not available.
1 = Closed caption data from field 1 is available.

CC field 2 available:

0 = Closed caption data from field 2 is not available.
1 = Closed caption data from field 2 is available.

WSS available:

0 = WSS data is not available.
1 = WSS data is available.

VPS available:

0 = VPS data is not available.
1 = VPS data is available.

VITC available:

0 = VITC data is not available.
1 = VITC data is available.

2.20.60 FIFO Word Count Register

Address	C7h

7	6	5	4	3	2	1	0
Number of words							

This register provides the number of words in the FIFO. 1 word equals 2 bytes.

2.20.61 FIFO Interrupt Threshold Register

Address	C8h
Default	80h

7	6	5	4	3	2	1	0
Number of words							

This register is programmed to trigger an interrupt when the number of words in the FIFO exceeds this value (default 80h). This interrupt must be enabled at address C1h. 1 word equals 2 bytes.

2.20.62 FIFO Reset Register

Address	C9h
Default	00h

7	6	5	4	3	2	1	0
Any data							

Writing any data to this register resets the FIFO and clears any data present.

2.20.63 Line Number Interrupt Register

Address	CAh
Default	00h

7	6	5	4	3	2	1	0
Field 1 enable	Field 2 enable	Line number					

This register is programmed to trigger an interrupt when the video line number matches this value in bits 5:0. This interrupt must be enabled at address C1h. The value of 0 or 1 does not generate an interrupt.

Field 1 enable:

0 = Disabled (default)
1 = Enabled

Field 2 enable:

0 = Disabled (default)
1 = Enabled

Line number: (default 00h)

2.20.64 Pixel Alignment Registers

Address	CBh	CCh
Default	4Eh	00h

Address	7	6	5	4	3	2	1	0
CBh	Switch pixel [7:0]							
CCh	Reserved						Switch pixel [9:8]	

These registers form a 10-bit horizontal pixel position from the falling edge of sync, where the VDP controller initiates the program from one line standard to the next line standard; for example, the previous line of teletext to the next line of closed caption. This value must be set so that the switch occurs after the previous transaction has cleared the delay in the VDP, but early enough to allow the new values to be programmed before the current settings are required.

2.20.65 FIFO Output Control Register

Address	CDh
Default	01h

7	6	5	4	3	2	1	0
Reserved							Host access enable

This register is programmed to allow I^2C access to the FIFO or allowing all VDP data to go out the video port.

Host access enable:

0 = Output FIFO data to the video output Y[9:2]
1 = Allow I^2C access to the FIFO data (default)

2.20.66 Full Field Enable Register

Address	CFh
Default	00h

7	6	5	4	3	2	1	0
Reserved							Full field enable

This register enables the full field mode. In this mode, all lines outside the vertical blank area and all lines in the line mode registers programmed with FFh are sliced with the definition of register FCh. Values other than FFh in the line mode registers allow a different slice mode for that particular line.

Full field enable:

0 = Disable full field mode (default)
1 = Enable full field mode

2.20.67 Line Mode Registers

Address	D0h	D1h−FBh
Default	00h	FFh

ADDRESS	7	6	5	4	3	2	1	0
D0h	Line 6 Field 1							
D1h	Line 6 Field 2							
D2h	Line 7 Field 1							
D3h	Line 7 Field 2							
D4h	Line 8 Field 1							
D5h	Line 8 Field 2							
D6h	Line 9 Field 1							
D7h	Line 9 Field 2							
D8h	Line 10 Field 1							
D9h	Line 10 Field 2							
DAh	Line 11 Field 1							
DBh	Line 11 Field 2							
DCh	Line 12 Field 1							
DDh	Line 12 Field 2							
DEh	Line 13 Field 1							
DFh	Line 13 Field 2							
E0h	Line 14 Field 1							
E1h	Line 14 Field 2							
E2h	Line 15 Field 1							
E3h	Line 15 Field 2							
E4h	Line 16 Field 1							
E5h	Line 16 Field 2							
E6h	Line 17 Field 1							
E7h	Line 17 Field 2							
E8h	Line 18 Field 1							
E9h	Line 18 Field 2							
EAh	Line 19 Field 1							
EBh	Line 19 Field 2							
ECh	Line 20 Field 1							
EDh	Line 20 Field 2							
EEh	Line 21 Field 1							
EFh	Line 21 Field 2							
F0h	Line 22 Field 1							
F1h	Line 22 Field 2							
F2h	Line 23 Field 1							
F3h	Line 23 Field 2							
F4h	Line 24 Field 1							
F5h	Line 24 Field 2							
F6h	Line 25 Field 1							
F7h	Line 25 Field 2							
F8h	Line 26 Field 1							
F9h	Line 26 Field 2							
FAh	Line 27 Field 1							
FBh	Line 27 Field 2							

These registers program the specific VBI standard at a specific line in the video field.

Bit 7:

0 = Disable filtering of null bytes in closed caption modes
1 = Enable filtering of null bytes in closed caption modes (default)

In teletext modes, bit 7 enables the data filter function for that particular line. If it is set to 0, then the data filter passes all data on that line.

Bit 6:

0 = Send VBI data to registers only.
1 = Send VBI data to FIFO and the registers. Teletext data only goes to FIFO. (default)

Bit 5:

0 = Allow VBI data with errors in the FIFO
1 = Do not allow VBI data with errors in the FIFO (default)

Bit 4:

0 = Do not enable error detection and correction
1 = Enable error detection and correction (when bits [3:0] = 1 2, 3, and 4 only) (default)

Bits [3:0]:

0000 = WST SECAM
0001 = WST PAL B
0010 = WST PAL C
0011 = WST NTSC
0100 = NABTS NTSC
0101 = TTX NTSC
0110 = CC PAL
0111 = CC NTSC
1000 = WSS PAL
1001 = WSS NTSC
1010 = VITC PAL
1011 = VITC NTSC
1100 = VPS PAL
1101 = Custom 1
1110 = Custom 2
1111 = Active video (VDP off) (default)

A value of FFh in the line mode registers is required for any line to be sliced as part of the full field mode.

2.20.68 Full Field Mode Register

Address	FCh
Default	7Fh

7	6	5	4	3	2	1	0
Full field mode							

This register programs the specific VBI standard for full field mode. It can be any VBI standard. Individual line settings take priority over the full field register. This allows each VBI line to be programmed independently but have the remaining lines in full field mode. The full field mode register has the same definitions as the line mode registers (default 7Fh).

3 Electrical Specifications

3.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (unless otherwise noted)†

Supply voltage range: IO_DVDD to DGND . . . . . −0.5 V to 4.5 V
DVDD to DGND . . . . . −0.5 V to 2.3 V
PLL_AVDD to PLL_AGND . . . . . −0.5 V to 2.3 V
CH_AVDD to CH_AGND . . . . . −0.5 V to 2.3 V
Digital input voltage range, V_I to DGND . . . . . −0.5 V to 4.5 V
Input voltage range, XTAL1 to PLL_GND . . . . . −0.5 V to 2.3 V
Analog input voltage range A_I to CH_AGND . . . . . −0.2 V to 2.0 V
Digital output voltage range, V_O to DGND . . . . . −0.5 V to 4.5 V
Operating free-air temperature, T_A . . . . . 0°C to 70°C
Storage temperature, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

3.2 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
IO_DVDD	Digital I/O supply voltage	3.0	3.3	3.6	V
DVDD	Digital supply voltage	1.65	1.8	2.0	V
PLL_AVDD	Analog PLL supply voltage	1.65	1.8	2.0	V
CH_AVDD	Analog core supply voltage	1.65	1.8	2.0	V
$V_{I(P-P)}$	Analog input voltage (ac-coupling necessary)	0		0.75	V
V_{IH}	Digital input voltage high	0.7 IO_DVDD			V
V_{IL}	Digital input voltage low			0.3 IO_DVDD	V
V_{IH_XTAL}	XTAL input voltage high	0.7 PLL_AVDD			V
V_{IL_XTAL}	XTAL input voltage low			0.3 PLL_AVDD	V
I_{OH}	High-level output current			2	mA
I_{OL}	Low-level output current			−2	mA
I_{OH_SCLK}	SCLK high-level output current			4	mA
I_{OL_SCLK}	SCLK low-level output current			−4	mA
T_A	Operating free-air temperature	0		70	°C

3.2.1 Crystal Specifications

CRYSTAL SPECIFICATIONS	MIN	NOM	MAX	UNIT
Frequency		14.31818		MHz
Frequency tolerance		±50		ppm

3.3 Electrical Characteristics

DVDD = 1.8 V, PLL_AVDD = 1.8 V, CH_AVDD = 1.8 V, IO_DVDD = 3.3 V

For minimum/maximum values: T_A = 0°C to 70°C, and for typical values: T_A = 25°C unless otherwise noted

3.3.1 DC Electrical Characteristics

PARAMETER		TEST CONDITIONS (see NOTE 1)	MIN	TYP	MAX	UNIT
$I_{DD(IO\_D)}$	3.3-V I/O digital supply current	Color bar input		4.8		mA
$I_{DD(D)}$	1.8-V digital supply current	Color bar input		25.3		mA
$I_{DD(PLL\_A)}$	1.8-V analog PLL supply current	Color bar input		5.4		mA
$I_{DD(CH\_A)}$	1.8-V analog core supply current	Color bar input		24.4		mA
P_{TOT}	Total power dissipation, normal mode	Color bar input		115	150	mW
P_{DOWN}	Total power dissipation, power-down mode (see Note 2)	Color bar input			1	mW
C_i	Input capacitance	By design		8		pF
V_{OH}	Output voltage high	I_{OH} = 2 mA	0.8 IO_DVDD			V
V_{OL}	Output voltage low	I_{OL} = −2 mA			0.22 IO_DVDD	V
V_{OH_SCLK}	SCLK output voltage high	I_{OH} = 4 mA	0.8 IO_DVDD			V
V_{OL_SCLK}	SCLK output voltage low	I_{OL} = −2 mA			0.22 IO_DVDD	V
I_{IH}	High-level input current	$V_I = V_{IH}$			±20	µA
I_{IL}	Low-level input current	$V_I = V_{IL}$			±20	µA

NOTES: 1. Measured with a load of 15 pF.
2. Assured by device characterization.

3.3.2 Analog Processing and A/D Converters

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Zi	Input impedance, analog video inputs	By design		500		kΩ
C_i	Input capacitance, analog video inputs	By design		10		pF
Vi(pp)	Input voltage range†	$C_{coupling}$ = 0.1 µF	0		0.75	V
ΔG	Gain control range		0		12	dB
DNL	DC differential nonlinearity	A/D only		±0.5		LSB
INL	DC integral nonlinearity	A/D only		±1		LSB
Fr	Frequency response	6 MHz		−0.9	−3	dB
SNR	Signal-to-noise ratio	6 MHz, 1.0 V_{P-P}		50		dB
NS	Noise spectrum	50% flat field		50		dB
DP	Differential phase			1.5		°
DG	Differential gain			0.5%		

† The 0.75-V maximum applies to the sync-chroma amplitude, not sync-white. The recommended termination resistors are 37.4 Ω as seen in Chapter 5.

3.3.3 Timing

3.3.3.1 Clocks, Video Data, Sync Timing

PARAMETER		TEST CONDITIONS (see NOTE 2)	MIN	TYP	MAX	UNIT
	Duty cycle PCLK			50%		
t_1	PCLK high time			18.5		ns
t_2	PCLK low time			18.5		ns
t_3	PCLK fall time	10% to 90%		4		ns
t_4	PCLK rise time	90% to 10%		4		ns
t_5	Output hold time		2			ns
t_6	Output delay time			3	8	ns

NOTE 3: Measured with a load of 15 pF.

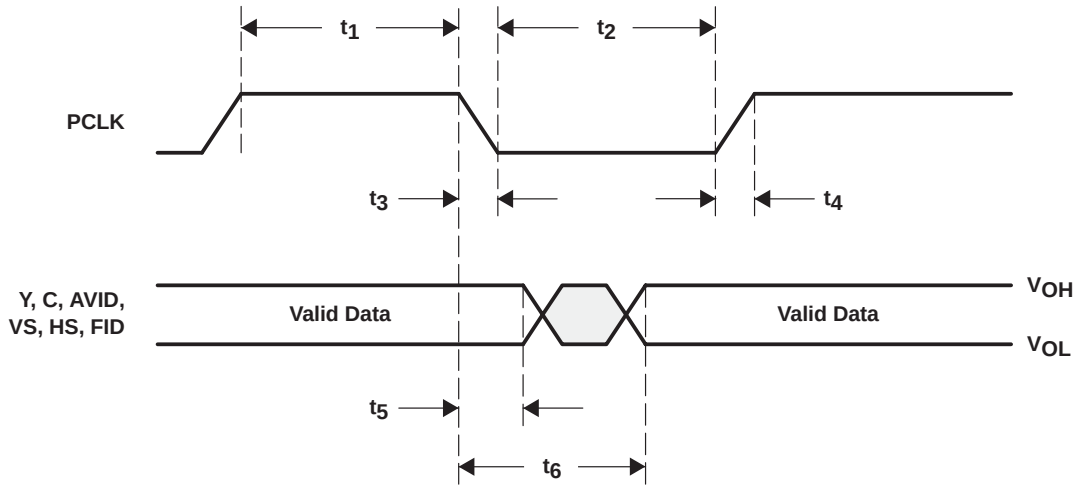


Figure 3−1. Clocks, Video Data, and Sync Timing

3.3.3.2 I^2C Host Port Timing

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Bus free time between STOP and START		1.3			µs
t_2	Setup time for a (repeated) START condition		0.6			µs
t_3	Hold time (repeated) START condition		0.6			µs
t_4	Setup time for a STOP condition		0.6			ns
t_5	Data setup time		100			ns
t_6	Data hold time		0		0.9	µs
t_7	Rise time VC1(SDA) and VC0(SCL) signal		250			ns
t_8	Fall time VC1(SDA) and VC0(SCL) signal			250		ns
C_b	Capacitive load for each bus line				400	pF
f_{I2C}	I^2C clock frequency				400	kHz

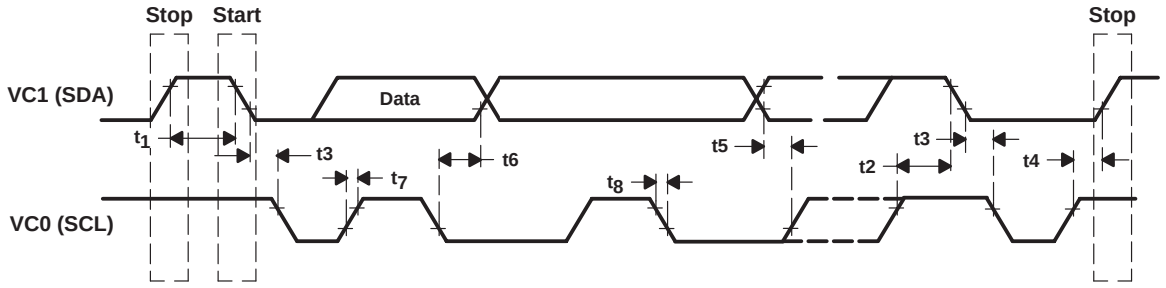


Figure 3–2. I^2C Host Port Timing

4 Example Register Settings

The following example register settings are provided only as a reference. These settings, given the assumed input connector, video format, and output format, set up the TVP5150A decoder and provide video output. Example register settings for other features and the VBI data processor are not provided here.

4.1 Example 1

4.1.1 Assumptions

Device: TVP5150AM1

Input connector: Composite (AIP1A)

Video format: NTSC-M, PAL (B, G, H, I), or SECAM

NOTE: NTSC-443, PAL-N, and PAL-M are masked from the autoswitch process by default. See the autoswitch mask register at address 04h.

Output format: 8-bit ITU-R BT.656 with embedded syncs

4.1.2 Recommended Settings

Recommended I^2C writes: For this setup, only one write is required. All other registers are set up by default.

I^2C register address 03h = Miscellaneous controls register address

I^2C data 09h = Enables YCbCr output and the clock output

NOTE: HSYNC, VSYNC/PALI, AVID, and FID/GLCO are high impedance by default. See the miscellaneous control register at address 03h.

4.2 Example 2

4.2.1 Assumptions

Device: TVP5150AM1

Input connector: S-video (AIP1A (luma), AIP1B (chroma))

Video format: NTSC-M, 443, PAL (B, G, H, I, M, N) or SECAM (B, D,G, K, KI, L)

Output format: 8-bit 4:2:2 YCbCr with discrete sync outputs

4.2.2 Recommended Settings

Recommended I^2C writes: This setup requires additional writes to output the discrete sync 4:2:2 data outputs, the HSYNC, and the VSYNC, and to autoswitch between all video formats mentioned above.

I^2C register address 00h = Video input source selection #1 register

I^2C data 01h = Selects the S-Video input, AIP1A (luma), and AIP1B (chroma)

I^2C register address 03h = Miscellaneous controls register address

I^2C data 0Dh = Enables the YCbCr output data, HSYNC, VSYNC/PALI, AVID, and FID/GLCO

I^2C register address 04h = Autoswitch mask register

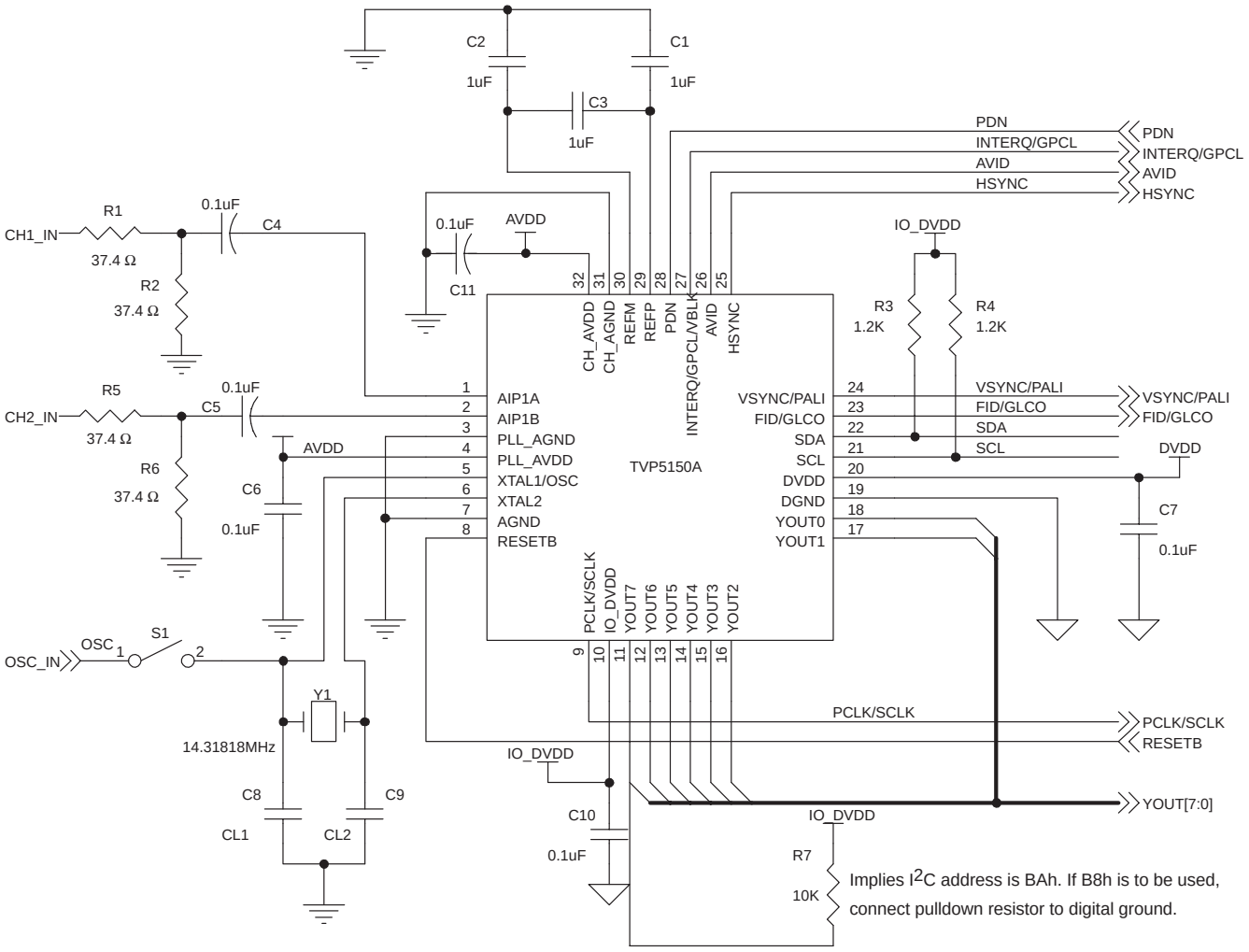
I^2C data C0h = Unmask NTSC-443, PAL-N, and PAL-M from the autoswitch process

I^2C register address 0Dh = Outputs and data rates select register

I^2C data 40h = Enables 8-bit 4:2:2 YCbCr with discrete sync output

5 Application Information

5.1 Application Example

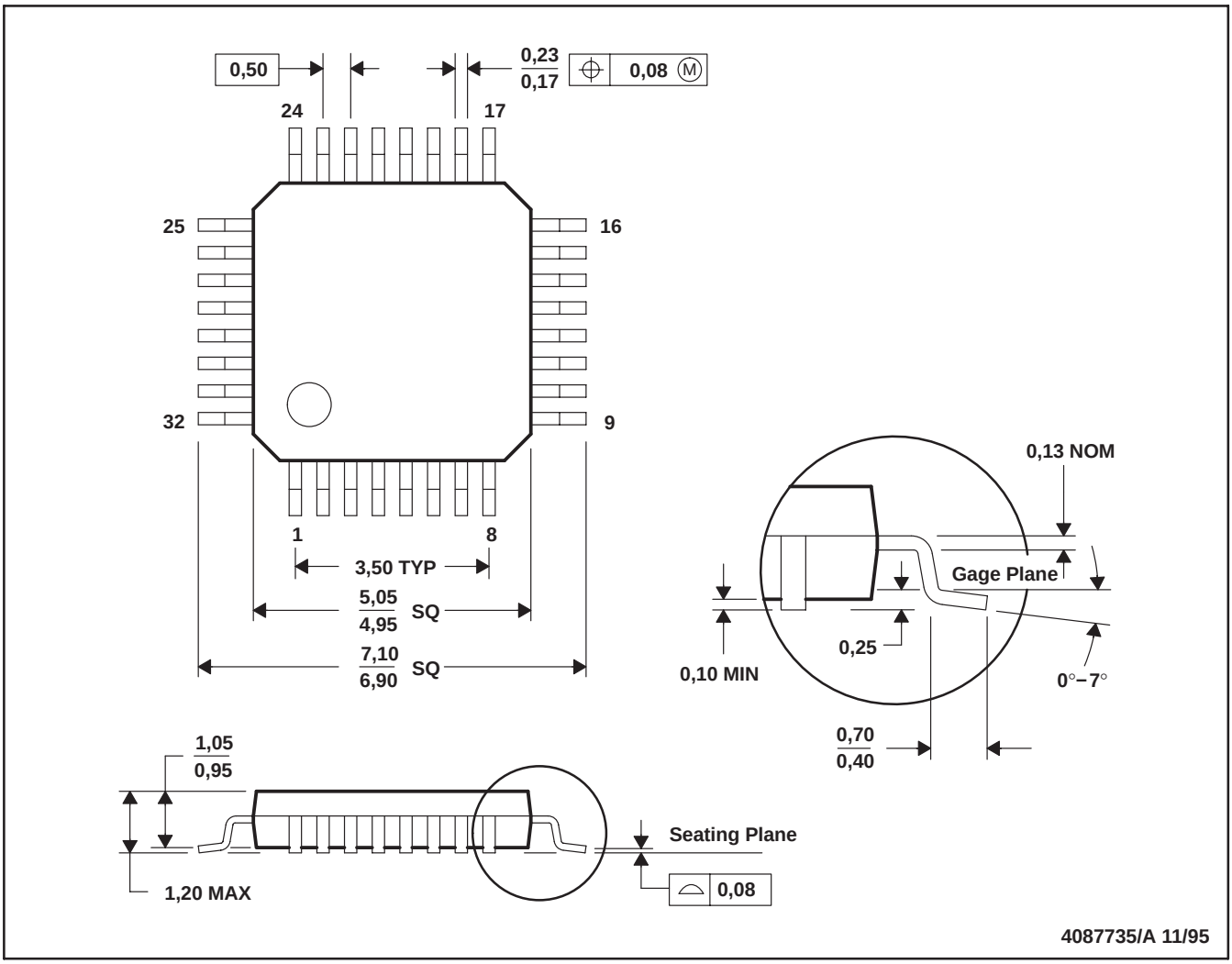


NOTE: The use of INTERQ/GPCL/AVID/HSYNC and VSYNC is optional. These are outputs and can be left floating.
When OSC is connected through S1, remove the capacitors for the crystal.
PDN needs to be high, if device has to be always operational.
RESETB is operational only when PDN is high. This allows an active low reset to the device.

Figure 5−1. Application Example

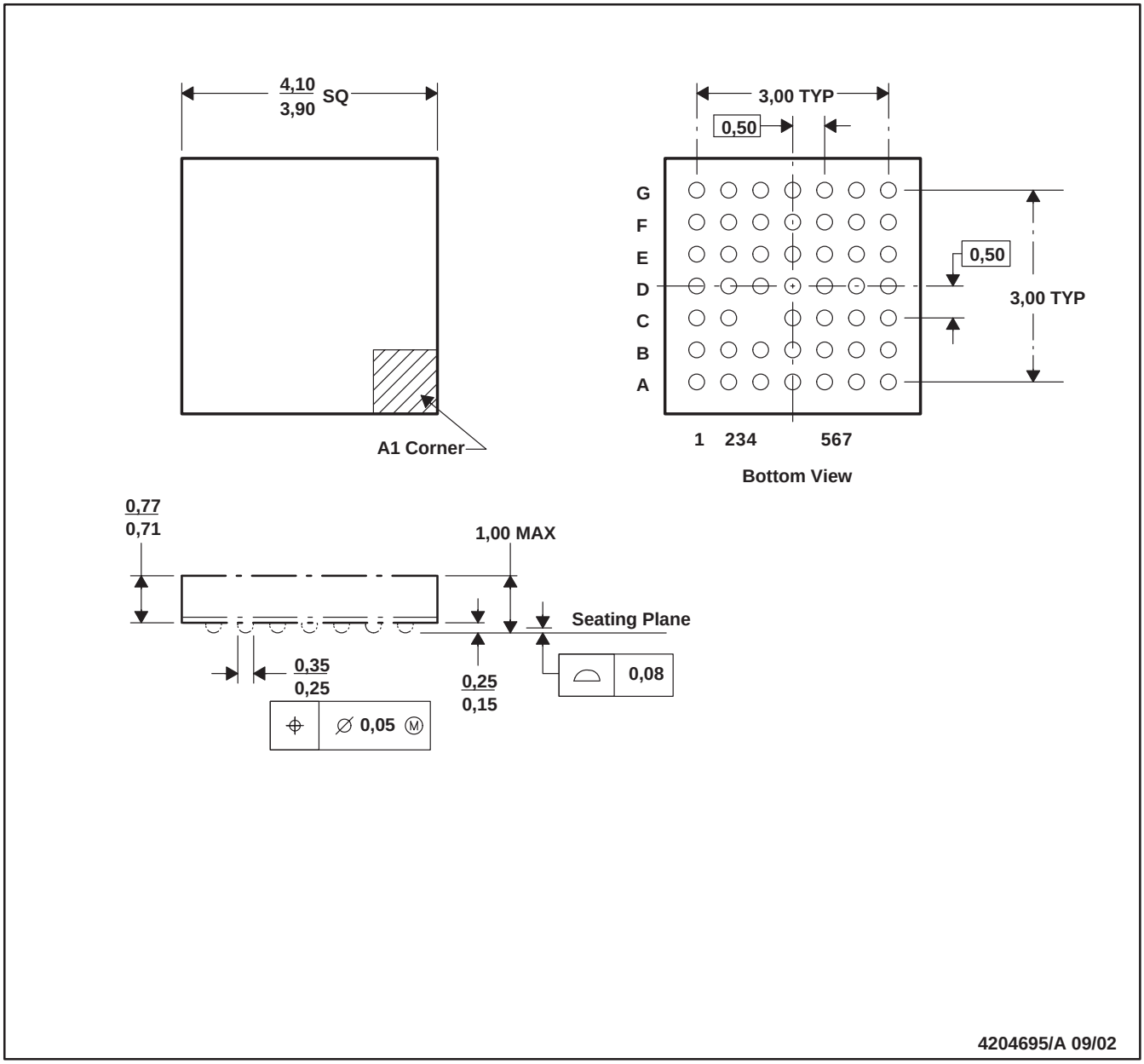
6 Mechanical Data

PBS (S-PQFP-G32) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

ZQC (S−PBGA−N48) **PLASTIC BALL GRID ARRAY**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar Junior™ BGA package configuration.
D. Falls within JEDEC MO-225
E. This package is lead free.

MicroStar Junior is a trademark of Texas Instruments.

PACKAGING INFORMATION

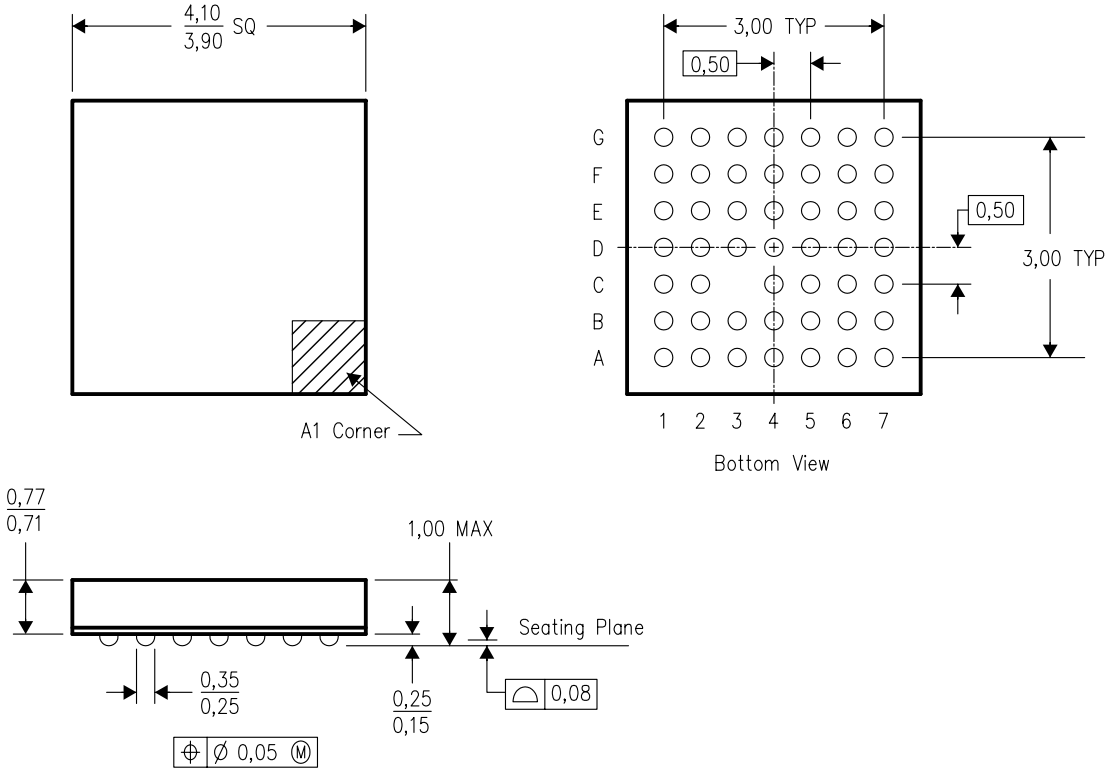
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TVP5150AM1PBS	ACTIVE	TQFP	PBS	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TVP5150AM1PBSR	ACTIVE	TQFP	PBS	32	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TVP5150AM1ZQC	ACTIVE	BGA MICROSTAR JUNIOR	ZQC	48	360	Pb-Free (RoHS)	SNAGCU	Level-3-260C-168 HR
TVP5150AM1ZQCR	ACTIVE	BGA MICROSTAR JUNIOR	ZQC	48	2500	Pb-Free (RoHS)	SNAGCU	Level-3-260C-168 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
None: Not yet available Lead (Pb-Free).
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

ZQC (S–PBGA–N48) PLASTIC BALL GRID ARRAY



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar Junior™ BGA configuration
D. Falls within JEDEC MO–225
E. This package is lead–free.

MicroStar Junior is a trademark of Texas Instruments.

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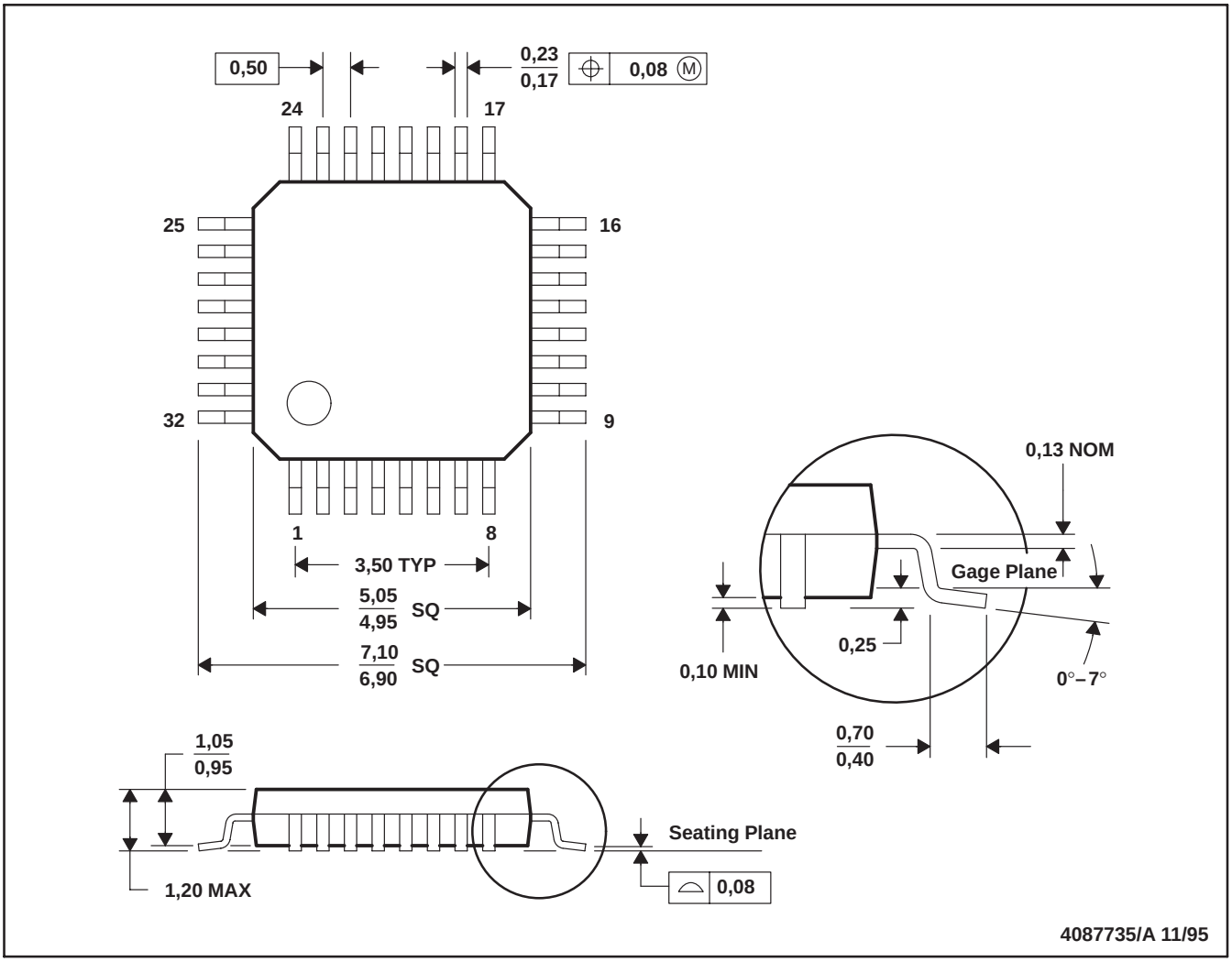
PBS (S-PQFP-G32) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.